Integrated Temperature and Current Controller for High Power LEDs Using Luminescent Lighting

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and

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Electrical Engineering

by

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Abstract

The usage of Light Emitting Diodes (LEDs) for lighting applications is significantly increasing. White light is the standard for these applications, it is divided in different types of light: cold white, neutral white and warm white depending on the application. Currently, there is no semiconductor material available emitting white light directly. Thus, other coloured LEDs are used and the emitted light of them is mixed to white light. As blue light emitting LEDs have the best efficiency today, they are the most promising base for white light. A part of the blue emitted light is converted into yellow light by a colour conversion layer placed on top of the semiconductor structure. The resulting mixture of both; the blue and the yellow light is recognised as white light by the human eye. By using this technique, a high efficient white LED can be realised. Nevertheless, LEDs still convert about 30 % to 90 % of power into heat. This power loss increases the LED device temperature which often results in a significant decrease of the lifetime of the LED and a colour shift or lumen reduction. Common design criteria of lights integrating LEDs lead to small size and low thermal conductivity, which enhances overheating of lighting systems. Therefore, a thermal management for LEDs is mandatory to ensure long life with constant light quality of the LED, which is the scope of this thesis. Part of this management is the determination of temperatures at different parts of the LED device. The sophisticated, complex and compact LED structures prevent a direct temperature measurement at key spots. A thermal-physical model of the LED is needed to determine temperatures at key points. Multiphysics simulations of typical LED structures are performed to develop a model of the thermal behaviour inside the LED. Results of the simulation are taken as basis for the development of a thermal measurement. The forward voltage of a p-n junction changes over temperature and can thus be used as an existing temperature sensor in the LED. Beside the semiconductor temperature, the temperature of the colour conversion layer need to be tracked too. Usually, the layer consist of phosphor embedded into silicone. Overheating changes the emitted colour of the phosphor and lumen loss can increase. For all these reasons a thermal management including temperature determination is developed. It is integrated into the LED driver and tested in a discreet development. Different approaches have been tested, evaluated and optimized using the discrete structure. The optimized approach was transferred in an Application-Specific Integrated Circuit (ASIC) design combining LED driver, temperature measurement and thermal management in a single chip to achieve a small size, low

cost highly integrated solution. The resulting chip controls the current of the LED while determining and controlling the LED temperature even at critical operation regions, which minimises risks of thermal hotspots.

Declaration

I hereby declare that this Ph.D. thesis entitled ”Integrated Temperature and Current Controller for High Power LEDs Using Luminescent Lighting” has been compiled by me, Thomas Tetzlaff, under the supervision of Prof. Dr. Ulf Witkowski.

This thesis has not been previously submitted for the award of any degree, diploma, associate-ship, fellowship or its equivalent to any other University or Institution.

Soest, March 2020

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Thomas Tetzlaff

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Special thanks go to my mother and my brother as well as my parents in law for their countless support. I wish I could discuss and share my results with my father who passed away too early during my Ph.D.. I hope he can read or recognise this work, wherever he may be now.

I dedicate this thesis to my wife Marie for her never-ending patience and indulgence over the last years. Thank you for being there even in darker days, laughing with me for countless hours and always keeping your heart open for me.

Contents

List of Figures

List of Tables

Acronyms

1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional
AAAS	American Association for the Advancement of Science
AC	Alternating Current
ACDM	Architecture Centric Design Method
ADC	Analogue To Digital Converter
Al_2O_3	Sapphire
AlGaInP	Aluminium Gallium Indium Phosphide
AlGaN	Aluminium Gallium Nitrate
AlN	Aluminium Nitride
ams	Austria Micro Systems
AMS	Austria Mixed Signal
AOT	Analogue On Top
ASIC	Application-Specific Integrated Circuit
ASIP	Application-Specific Instruction-set Processors
ASM	Analogue Simulation and Modelling
ATPG	Automatic Target Generation Process
BIOS	Basic Input Output System
CCM	Continuous Current Mode
CDC	Clock Domain Crossing
CMOS	Complementary Metal Oxide Semiconductor
CRI	Colour Rendering Index
CPM	Critical Path Monitor

CTS	Clock Tree Synthesis
DAC	Digital To Analogue Converter
DOT	Digital On Top
DC	Direct Current
DCM	Discontinuous Current Mode
DH	Double Heterostructure
DRC	Design Rule Check
DTM	Dynamic Thermal Management
DTS	Digital Temperature Sensor
EoL	End of Life
ESD	Electrostatic Discharge
FET	File Effect Transistor
FEV	Front End and Verification Suite
FPA	focal plane array
FPGA	Field Programmable Gate Array
GaInN	Gallium Indium Nitride
GaN	Gallium Nitrate
GUI	Graphical User Interface
HDL	Hardware Description Language
HDMI	High Definition Multimedia Interface
hitkit	High Performance Interface Tool Kit
HP-LED	High-power Light Emitting Diode
HY	Hybrid
IBM	International Business Machines Corporation
IC	Integrated Circuit
IDBB	Integrated Double Buck Boost
IESNA	Illuminating Engineering Society of North America
IMP	Implementation Suite

InGaN	Indium Gallium Nitrate
InSb	Indium Antimonide
IP	Intellectual Property
IQE	Internal Quantum Efficiency
IR	Infrared
LCD	Liquid-Crystal Display
LED	Light Emitting Diode
LQR	Linear Quadratic Regulator
LUT	Look Up Table
LVS	Layout Versus Schematic
MCPCB	Metal-Core Printed Circuit Boards
MODGEN	Module Generator
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPC	Model Predictive Control
MQW	Multiple Quantum Well
MSOT	Mixed Signal On Top
MSPS	Mega Sample Per Second
NVM	Non Volatile Memory
OP-AMP	Operational Amplifier
PCB	Printed Circuit Board
PCell	Parametrized Cell
PDK	Process Design Kit
PECI	Platform Environment Control Interface
PEL	Presuppositions Evidence and Logic
PF	Power Factor
PID	Proportional Integral Derivative
PJTM	Pulsed Junction Temperature Measurement
PLL	Phase Locked Loop

PMOS	P-Type Metal-Oxide-Semiconductor
POSMDP	Partially Observable Semi-Markov Decision Process
PRS-LED	Photon-recycling Semiconductor LED
PSL	Property Specification Language
PWM	Pulse Width Modulation
QD	Quantum Dot
QW	Quantum Well
RCLK	Register Clock
RF	Radio Frequency
RGB	Red, Green and Blue
RTL	Register Transfer Language
SAR	Successive Approximation Register
SDC	Synopsys Design Constraint
Si	Silicon
SiC	Silicon Carbide
SMDP	Semi-Markov Decision Process
SOC	System On Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
SRH	Shockley Read Hall
SSADM	Structured Systems Analysis and Design Method
SVA	SystemVerilog Assertions
SYSL	System Level
TAU	Thermal Assist Unit
TCAD	Technology Computer Aided Design
TCM	Temperature Controlled Mount
TDP	Thermal Design Point
TI	Texas Instruments
TM	Thermal Monitor

TM1	Thermal Monitor1
TM2	Thermal Monitor2
TP	Transition Probability
TPMD	Thermal and Power Management Device
TTE	Thermal Transient Effect
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
V-Model	Validation and Verification Model
VHDCI	Very High Density Cable Interconnect
VHDL	Very High Speed Integrated Circuit Hardware Description Language
ZnSe	Zinc Selenide

List of own Publications

[1] T. Tetzlaff and U. Witkowski, “Current load capacity of electrical conductor tracks evaluated by simulation and thermographic imaging,” in *2015 16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, April 2015, pp. 1–5.

[2] T. Tetzlaff, M. A. A. B., and U. Witkowski, “Estimation of led junction temperature based on forward voltage method for digital hardware implementation,” in *2016 European Modelling Symposium (EMS)*, Nov 2016, pp. 223–228.

[3] T. Tetzlaff and U. Witkowski, “Digital hardware implementation of led temperature measurement based on forward voltage method,” in *2017 European Modelling Symposium (EMS)*. IEEE, 2017, pp. 255–259.

[4] T. Tetzlaff and U. Witkowski, “Hardware implementation of led forward voltage measurement for junction temperature estimation,” in *2018 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*. IEEE, 2018, pp. 1–5.

1

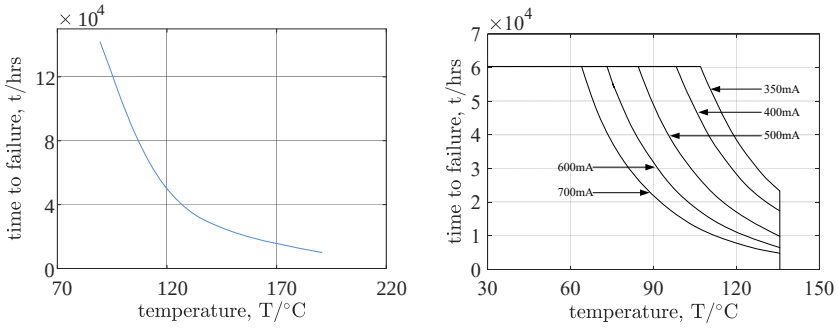
Introduction

See first, think later, then test. But always see first.
Otherwise you will only see what you were expecting.
Most scientists forget that.

Douglas Adams

White light Light Emitting Diodes (LEDs) have been replacing traditional light sources such as light bulbs and neon tubes since their market launch in 1995 [1]. They are commonly used for street lighting [2] and in the last years they are used not only for car back lights, but also for car front lights [3]. Efficiency and luminous output of LEDs have been significantly increased during the last decade reaching from 100 lm W^{-1} [4] to more than 150 lm W^{-1} [5, 6] and counting. Compared to classical light sources, such as fluorescent bulbs (105 lm W^{-1}), metal halide (122 lm W^{-1}) and high-pressure sodium vapour lamps (150 lm W^{-1})[5], their efficiency is quite good or even better. In contrast to traditional light sources, LED efficiency and light quality are significantly improving. Hence, they are replacing more and more traditional lights with high demand of energy, such as Liquid-Crystal Displays (LCDs), general-purpose luminaries and video projectors [7–9]. In 2005 6.5 % of the global primary energy was used for lighting [10]. By changing 86 % of the main light source from classic to LED, the USA can save approximately 75 % of the used electric power for lighting by 2035 [11].

Nevertheless, LEDs still convert about 30 % to 90 % of power into heat [12]. Beside the unavoidable energy waste, the related self-heating of LEDs usually results in a decrease of lifetime by up to 20 %. Most of current LED ageing and lifetime prediction methods are base on a relationship of luminous flux, temperature and current [13–15]. Parameters of the lifetime prediction methods are fitted using accelerated lifetime prediction tests. These tests use high currents and temperatures to accelerate the ageing of



(a) (b)

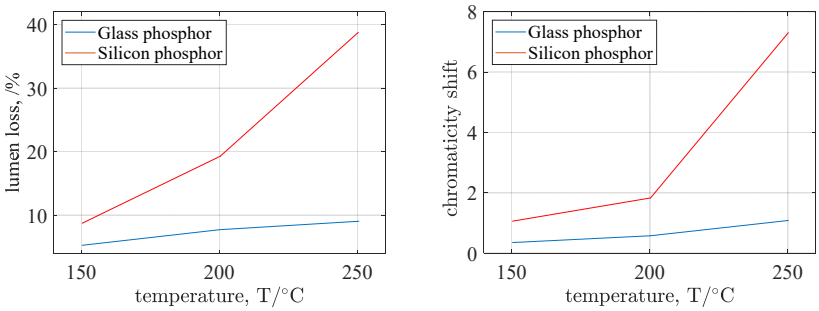
Figure 1.1: Time to failure (70 % lumen reduction) versus temperature with a maximum operation temperature of 90 °C [20] (a). Lifetime test of a Philips Luxeon Rebel RD07 at different temperatures provoked by rising supply current [21] (b). A minor change in temperature will result in a major change of lifetime

LEDs [16–20]. For example Yazdan Mehr et al. [20] describe an acceleration factor A which is defined only by the temperature:

$$A = \frac{E_a}{k\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \tag{1.1}$$

Where E_a is the activation energy [eV], k is a constant [eV K^{-1}] to be calibrated for the LED type, T_1 is the maximum operation temperature and T_2 is the current temperature. The higher the difference between maximum working temperature and the current temperature of the LED, the lower the lifetime. Figure 1.1 indicates the relation between temperature and lifetime graphically. It can be seen that even a minor change in temperature will result in a major change of lifetime. Similar results were observed by Lall et al. [22] who performed experimental tests on a commercial phosphor converter LED where the relative luminous flux of one LED is reduced by 30 % after the LED was heated to 175 °C for 2000 h. In addition, Efremov et al. [23] stated a reduction of efficiency of up to 30 %. The Illuminating Engineering Society of North America (IESNA) developed a temperature based ageing standard LM-80 [24]. This standard test allows to evaluate lumen maintenance of LEDs by ageing them at three predefined temperatures.

After ageing, the LED is cooled down to room temperature and thus bolometric as well as photometric tests are performed. Therefore, it is crucial to identify the temperature of the active region of the LED. Methods determining and analysing the LED temperature are widely discussed



(a) (b)

Figure 1.2: Lumen loss as a function of ageing temperatures [30](a) and chromaticity shift as a function of ageing temperatures [30](b) both of glass and silicon phosphor

in the literature [25–29]. Most of the tests and developments are based on simulation results and are not applied to real LEDs in operation. The speed and accuracy of the methods where not tested on LEDs. The implementation for real time temperature determination was neither performed nor analysed.

Additionally, current high power white LEDs are based on blue LEDs with a colour conversion layer on top. This colour conversion layer consists of glass or silicon phosphor in most cases. High temperatures in this layer cause lumen loss and a chromaticity shift [30]. Lumen loss decreases the light output of the LED which reduces the efficiency of the entire lighting device, while the chromaticity shift will change the colour of the LED light and thus the light quality. Figure 1.2 indicates how the light efficiency and the light quality change for glass and silicon phosphor type LEDs. The measured values of the lumen loss and chromaticity shift are also listed in Table 1.1. It can be seen, that glass-based phosphor has a better temperature stability compared to silicon phosphor. Lumen loss of glass-based phosphor is 1.7, 2.8, and 4.8 times less compared to silicon-based phosphor and shows 3.1, 3.3, and 6.8 times less shift in chromaticity. The results of this study are supported by similar results from Ryu and Ryu [31]. It is also important to know the temperature of the phosphor to reduce or even avoid overheating and fast ageing. Besides knowing the thermal effects of the phosphor layer, there is no method known to determine the temperature of the phosphor layer. Thermal analysis of the layer as shown in Figure 1.2 and Table 1.1 are based on experiments where the phosphor is placed in a heating chamber to simulate high temperature ageing. Only a few works discuss the thermal interaction between active region and phosphor layer [32–34]

Currently there is no LED driver including an applicable temperature

Table 1.1: Lumen loss and chromaticity shift of glass and silicon phosphor at 150 °C, 200 °C and 250 °C [30]

	temperature	150 °C	200 °C	250 °C
lumen loss	glass phosphor	4.2 %	6.7 %	8.2 %
	silicon phosphor	7.7 %	18.7 %	38.9 %
chromaticity shift	glass phosphor	1.0	1.8	7.3
	silicon phosphor	0.4	0.6	1.1

measurement with sufficient speed and accuracy on the market. There are some driver using an external temperature-sensitive resistor measuring the PCB temperature [35]. This temperature is used to estimate the LED temperature. Due to the complex structure of current LEDs and variations in solder technologies, the estimation is inaccurate. The thermal low-pass filter behaviour of the PCB and LED structure cannot detect temperature changes as fast as they occur. Furthermore, there is no driver with an approved thermal management for LEDs. Literature discusses the attachment of a heat sink as thermal management for LEDs [36–42]. The motivation of this thesis is to develop a methodology to detect the temperature of the active region of the LED, as well as the temperature of the phosphor layer. Although, methods exist detecting the temperature of the active region, they have to be analysed and tested in an experimental setup and the speed and accuracy has to be figured out. There is no method for the phosphor temperature determination. It has to be analysed whether a method for junction temperature determination can be used to detect the phosphor temperature. To achieve this multiphysic simulations of LEDs, the thermal distribution in the LED has to be detected. In addition to temperature determination an active thermal management is needed to avoid overheating and to enable a maximum lifetime of the LED. A main requirement of the work is that the functionalities should be integrable into the LED driver in an optimised way. A temperature determination method with minimum resources has to be identified or developed as well as a thermal management.

In addition to an internal Dynamic Thermal Management (DTM) external cooling needs to be applied to the LED. Current LED systems are cooled using a simple heat sink attached to the LED. By knowing the actual temperature of the LED, external active cooling can be controlled too. Some novel active low noise cooling technologies are discussed in literature which can be combined with an internal thermal management. Using a temperature output of the thermal management an additional external control system can be applied. Goal is an LED system keeping track of the LED temperature. The system reacts fast to temperature changes using

adopted forward current. Additionally, an external active cooling system is needed trying to keep the light output on its desired value.

The general objective of this research project is to design an optimised thermal LED management which controls the LED operation point in order to maximise the lifetime of LEDs. The work comprises two parts. The first part is aimed at measuring and controlling LED temperature. For this purpose, the temperatures of the luminescent material as well as the semiconductor junction have to be determined. It is planned to develop a simplified mathematical model derived from data of multiphysics simulations of the electric-thermal behaviour of LED. An overview of current cooling systems and their efficiency and usability in LED technology are included as well. The second part of the thesis is the design of an Application-Specific Integrated Circuit (ASIC) with an optimal set-up of hardware and data processing algorithms including the temperature controller. By integrating the ASIC into the LED driver system, a small size and robust lighting system is designed. With a low power consumption and good performance, with respect to temperature control, thermal stress inside the LED structure is reduced and the LED lifetime is increased.

1.1. Research Method

This section introduces available research methods and describes what they are used for. Applicable methods for this project are described and one method is chosen to be used in this work. A precondition is that a research method, often misrepresented, is not a fixed sequence of steps. It is more like a highly variable creative process [43]. Thus, scientific research has general principles which have to be mastered to increase productivity and enhance hyperactivity, no simple automated sequence of steps is available to follow [44]. In most textbooks about scientific research, the elementary science methods are defined in the following steps:

- Hypothesis formation
- Hypothesis testing
- Deductive and induction logic
- Controlled experiments; replication and repeatability
- Interactions between data and theory
- Limits to science's domain

But scientific research goes beyond these steps. The American Association for the Advancement of Science (AAAS) describes the scientific methodology as a combination of general principles and specialised techniques. "Some important themes pervade science, mathematics, and technology and appear over and over again, whether we are looking at an ancient civilization, the human body, or a comet. They are ideas that transcend disciplinary boundaries and prove fruitful in explanation, in theory,

in observation, and in design"[45]. Researchers and scientists basically claim four principals: rationality, truth, objectivity and realism. There are also other claims discussed which can be described as a variation of those four claims. Rationality is a good argument. "Pieces of behaviour, beliefs, arguments, policies, and other exercises of the human mind may all be described as rational. To accept something as rational is to accept it as making sense, as appropriate, or required, or in accordance with some acknowledged goal, such as aiming at truth or aiming at the good"[46]. Truth of a statement occupies the correspondent with reality. The theory of truth goes back to Aristotle who said that "To say of what is that it is not, or of what is not that it is, is false, while to say of what is that it is, and of what is not that it is not, is true"[47]. Objectivity often appears as adjectives, as objective belief, objective knowledge or objective truth. It can be described by the objective knowledge of something, i.e. table salt is sodium chloride. To conclude the four principle claims, realism is defined as: "Scientific realism embodies the claim that the scientific method provides rational access to physical reality, generating much objective knowledge. Realistic beliefs correspond with reality"[43]. Gauch [43] describes the following methods for scientific research, which can be used individual or in a mixed way.

- The scientific method of common sense
- The Presuppositions Evidence and Logic (PEL) model of full disclosure
- Disclosure of Presuppositions

The concept of scientific research according to Thomas Reid is based on common sense. It has five main elements: the symmetry thesis, harmonious faculties, parity among presuppositions, reason's double office mean and ask twice. The symmetry thesis which equals the priority and status as internal and external. Harmonious faculties, which Reid confirms to be the basic reliability of all faculties, are sensory and mental. Parity among presuppositions is where a parity between realist and sceptical presuppositions should be achieved. Reason's double office mean that belief and action should match. If not, the scientific results could be only based on the mismatch between belief and action. If a question is asked twice, a deeper issue can be detected by using greater resources [43].

The Presuppositions Evidence and Logic (PEL) model of full disclosure uses a presupposition added to evidence and logic which draws a conclusion. It starts with presuppositions, which are beliefs that are necessary for the hypotheses, for example that the physical world exists. Evidence must be meaningful for the hypotheses and proven with data. To reach a conclusion, the logic is used to combine presupposition and evidential premises.

The disclosure of the presuppositions method is based on two steps. The first step, called reality check, is a certain common-sense knowledge

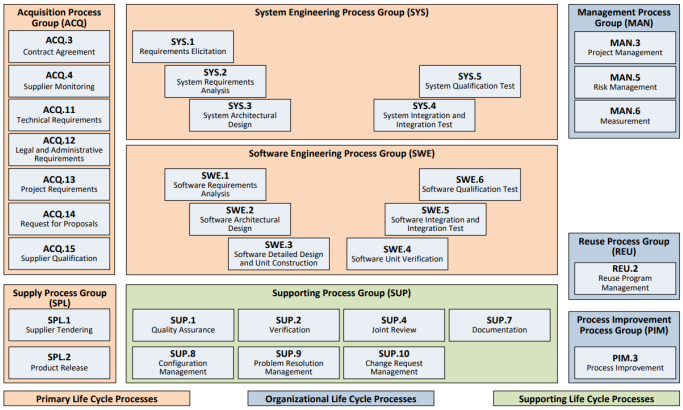


Figure 1.3: Automotive SPICE process reference model - Overview [48]

about the world is selected. Secondly, the philosophical reflection track down its presuppositions shows that they are sufficient for scientific thinking.

In addition to that, Gauch [43] names two important rules of engagement; first a clearly defined target and second rhetoric and substance. To identify applicable research methods for the stated problem, the type of research has to be identified. Possible types of research are descriptive, analytical,applied, fundamental,qualitative, quantitative conceptual, empirical or a mix of the stated types [49]. This engineering work can be described as a mix of applied and conceptual types with a combination of laboratory and simulation research. Thus, for this work the PEL model of full disclosure is used. To present a scientific conclusion with full disclosure presuppositions, evidence and logic has to be combined. Since these three components have a powerful interaction, they need to be understood and defined together.

This work also includes a system design. The system design is performed to demonstrate the functionality of the theoretical ideas and developed approaches empirically. Standard engineering system development method was the waterfall method [50]. The waterfall method is a sequential method of steps where each step must be completed and frozen before the next step can be started. No feedback from different steps is possible. Therefore, no pretesting of individual parts rather no adoption to new outcomes is possible. To overcome this fact software design methods like Structured Systems Analysis and Design Method (SSADM) [51], Architecture Centric Design Method (ACDM) [52] or Validation and Verification Model (V-Model) [53] are adopted to fit engineering systems design. One industry used standard is Automotive SPICE [48], which is

base on the V-Model and combines software and hardware engineering processes as well as management, supporting and supervision processes, cf. Figure 1.3.

In this work the software and hardware part of Automotive SPICE is used. Both, the hardware development and the software development is performed using a reduced V-Model. This concept allows to validate and verify parts of the development before continuing to the next step. Especially for the new developed methodologies it is mandatory to test and validate parts of the development. In addition, requirements can change due to results from validation and testing. In the V-Model also changes in requirements are possible in the development phase.

1.2. Outline Of The Thesis

This chapter introduces the thesis and gives information about LED ageing and its effect.

Chapter 2 starts with an introduction to white light LEDs with the semiconductor basic theory. After describing possible ways of white light creation with LEDs, current structures of LEDs are presented. Layer sets of active regions of LEDs are described with the dome of the LED. The structure part is concluded by showing LED package types. The next part of the chapter focuses on the LED temperature. A classical thermal model for LEDs is introduced as well as novel theories which detect or determine the temperature of the active region of an LED without using external measurements. The best fit theory needs to be calibrated for each LED type, therefore the calibration process is also shown in this chapter. Beside the temperature of the active region, it might be important to know other temperatures in the LED. To identify these temperatures, multiphysic simulations of LEDs are shown and the results are discussed. When the temperature of the LED is known, it needs to be cooled. For this purpose, classic cooling methods and upcoming low noise cooling methods are introduced. Usability and cooling of low noise methods are validated by experiments. To conclude Chapter 2 possible applicable DTMs are presented.

Chapter 3 lists possible ways to supply LEDs. Starting by listing classic driver topologies with their advantages and disadvantages, new approaches with a high power factor and inductor less drives are discussed. After identifying a possible driver which can be used in this work, a current controller is designed for the driver. For the controller development two different model identification methods are used. A system average model and the system identification of MATLAB®. The controller is tested in the simulation environment SPICE

The following chapter of this thesis are focused on implementation, optimisation and testing of the previously developed methods. Chapter 4

describes a discrete system using a development board with self developed extinctive board. Purpose of this discrete system is the test and optimization of the LED driver, the temperature determination and the DTM.

With a working test system and a developed code which can also be used for chip design, the entire discrete system was integrated into an ASIC in Chapter 5. Finally, the ASIC was taped out and assembled. The finished chip was tested and validated with test PCB described in Chapter 6. Conclusions about this study and interesting ideas for future research are finally discussed in Chapter 7.

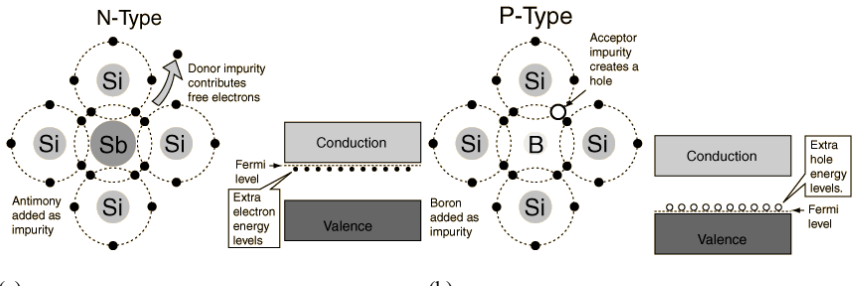
2

Light Emitting Diode (LED)

Nothing travels faster than the speed of light
with the possible exception of bad news,
which obeys its own special laws.

Douglas Adams

This chapter gives an overview of current white light LEDs. It begins by introducing the possibilities to generate white light using LEDs and shows which type is the most applicable for lighting applications. Semiconductor structures used in the active region of LEDs discussed in current literature are introduced and it is shown how they improve their efficiency. Furthermore, package types of LEDs are listed and their heat dissipation behaviour is analysed. Followed by information about thermal losses inside the LED and their negative effects to the LED, LED self heating is described including methodologies to identify the LED chip temperature. These methodologies are compared and evaluated in therms of their integrability. The most applicable method is validated and the variations are identified and tested as well as compared by experiments. Multiphysic simulations are performed to identify thermal hot-spots within the LED. Starting by simulating the active region, more complex simulations of a complete LED including package and dome are performed. Two different placements of phosphor and their thermal behaviour are simulated and compared. Multiphysic simulations are concluded by a simulation of a CREE® LED to identify the temperature of the chip and the phosphor. The results of the simulation are compared to experimental measurements. For these experiments the temperature of an LED is recorded by an infrared camera. Subsequently, cooling mechanism for LEDs are introduced and characterised. In addition to classical cooling methods, such as heat sink with attached fan, new low-noise cooling methods are listed and tested. Part of the low-noise cooling technologies are ionic winds and synthetic



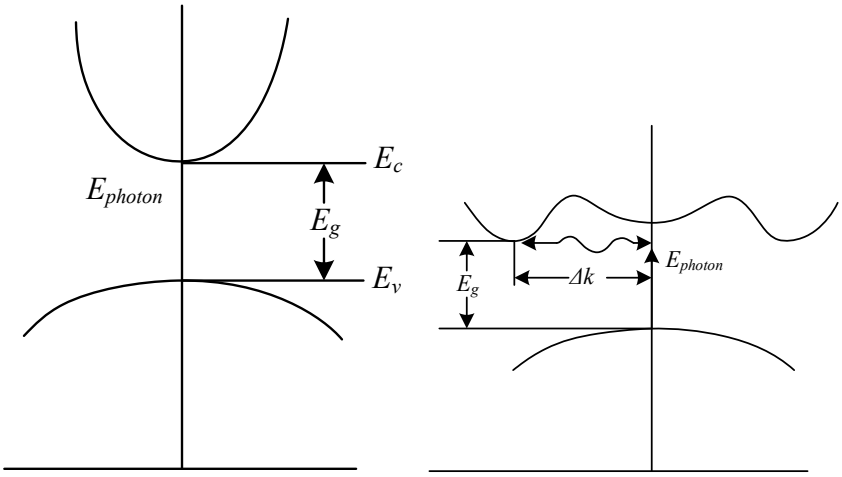
(a) (b)

Figure 2.1: Atomic structure example of an n-type (impurity: antimony-Sb) (a) and p-type (impurity: boron-B) semiconductor using silicon (b) [54]

jets which have been analysed in detail performing experimental tests. To conclude this chapter, thermal management techniques for semiconductors are described and possible variations to use these in LED applications are developed.

2.1. Semiconductor Basic Theory

Materials can be classified in conductors, insulators and semiconductors. The semiconductors are characterised by a small gap (i.e. Energy band gap or E_g) between the energy states (i.e. between the energy bands). The energy bands are the conduction band and the valence band; different processes are presented between these bands. Another important parameter is the Fermi level; it describes the top of the available electron energy levels at 0 K and its position with respect to the conduction band which is important for electrical properties [54]. The basic structure on which the LEDs are based is the p-n junction; this junction is composed of two types of semiconductors. These types are formed by the addition of foreign atoms (i.e. doping). For n-types it will contribute free electrons and for p-types, the addition produces a deficiency of electrons in the valence band known as holes. The principle of doping is shown in Figure 2.1. The pure material is called intrinsic. The semiconductors can also be classified according to the band structure in indirect and direct band gaps. To understand these concepts, the energy is defined as a function of a wave vector k which defines the crystal momentum. When the crystal momentum of both bands is the same, the material has a direct band gap and when it is different, the material has indirect band gap which is depicted in Figure 2.2 [55]. To obtain more efficiency and output power, the LEDs are based on direct band gap semiconductors. The Energy Band gap E_g for direct band gap materials is equal to the sum of the Photon Energy E_{photon} and



(a) (b)

Figure 2.2: Energy band diagram for a direct band gap (a) and for an indirect band gap (b) [55]

for indirect band gap is equal to the Photon energy and the Phonon energy ($E_{photon} + E_{phonon}$). To define the wavelength in which a semiconductor produces light, the Planck Einstein relation is introduced [56]:

$$\lambda = \frac{h \cdot c}{E_g} = \frac{1240}{E_g} \tag{2.1}$$

Where λ is the wavelength of the light, h is the Planck constant, c is the speed of light and E_g is the photon energy. In a p-n junction two types of currents can be found (i.e. diffusion and drift currents). The diffusion current is the result of the concentration gradient from a higher concentration area to a lower concentration area and drift current is caused by the motion of charges as a result of an applied electric field. The diodes can work in forward and reverse biased modes. For this work, the forward bias mode is the most important one, an LED is operated in this mode where the electron current flows from the n-type to the p-type. A modification of the p-n normal diode is the p-i-n diode in which an intrinsic region is located between the n and p type semiconductors. In the new layer, a space charge region is included which is initially depleted of mobile charges. In unbiased mode, the diffusion current and the drift current are in balance. After applying an external voltage, this balance is affected and produces a current flux [57]. The current-voltage behaviour of the semiconductor

diode can be defined by the Shockley ideal diode equation [56]:

$$I = I_S \cdot \left(e^{\frac{V_D}{n \cdot V_T}} - 1 \right) \tag{2.2}$$

$$V_T = \frac{k \cdot T}{q} \tag{2.3}$$

Where I is the diode current, I_S is the reverse bias saturation current, V_D is the voltage across the diode, V_T is the thermal voltage, n is the ideality factor, k is the Boltzmann constant, T is the absolute temperature of the p–n junction and q is the magnitude of charge of an electron. To better understand the LED processes related to light generation, which is the product of recombination processes, the different types of recombination are introduced, as following:

- Band to band: electron of the conduction band falls in a hole of the valence band. Generally a radiative recombination occurs [56].
- Shockley Read Hall (SRH) recombination or trap assisted: when an electron falls into a trap at an energy level between the conduction and valence bands. The trap is caused by an impurity or a structural defect. The trap only accepts one electron, which can recombine later in the valence band [56].
- Auger recombination: electron and hole recombine in a band to band transition, but the energy is not translated into a photon, it is given to another electron or hole [56].

To increase the recombination rates, it is desirable that the carriers recombine in a region with high carrier concentration. For this reason, a structure is needed which is able to confine carriers in a small region (i.e. active region). This narrow region is achieved by using semiconductors of a narrow bandgap (e.g. approximately 2.7 eV for Indium Gallium Nitrate (InGaN) in the active region). When the active region composes a Double Heterostructure (DH) with a thickness similar to the Broglie wavelength of the carriers it is called Quantum Well (QW) (i.e. thickness must be less than 20 nm). The Shockley diode equation for an ideal diode is given with the premise that the current is the result of drift, diffusion and thermal recombination-regeneration processes. However, other processes such as photon recombination and generation are not considered [56]. The n factor of (2.2) with value 1 represents a diode with radiative recombination only and for $n > 1$ it includes the non-radiative recombination [57]. To understand the LED structures, their processes and performance, the Shockley equations for semiconductors are used, which govern the drift, diffusion and generation-recombination-trapping-detrapping of electrons

and holes, these are [58]:

$$q \cdot \left(\frac{\partial n}{\partial t}\right) = +\nabla j_N + q \cdot (g_N - r_N) \tag{2.4}$$

$$q \cdot \left(\frac{\partial p}{\partial t}\right) = -\nabla j_P + q \cdot (g_P - r_P) \tag{2.5}$$

$$j_N = +q \cdot \mu_n \cdot n \cdot E - q \cdot D_n \cdot \nabla n \tag{2.6}$$

$$j_P = +q \cdot \mu_p \cdot p \cdot E + q \cdot D_p \cdot \nabla p \tag{2.7}$$

$$\nabla \cdot \varepsilon E = q \cdot (p - n + N_{DD} - N_{AA} - n_T) \tag{2.8}$$

$$\frac{\partial n_T}{\partial t} = (g_P - r_P) - (g_N - r_N) \tag{2.9}$$

(2.4) and (2.5) are the continuity equations of electrons and holes. (2.6) and (2.7) are the electron and hole current-density equations, (2.8) is the Poisson equation which expresses the change of electric field related to the volume charge density [58]. (2.9) defines the rate of trapped electron concentration (or trapped hole concentration). The current-density equations are defined by the drift and diffusion components (2.6) and (2.7). The continuity equations are defined in terms of the electron and hole generation rate (g_N and g_P, which are caused by external influence as high energy photons or impact ionisation under large electric fields) and the electron and hole recombination rates (r_N and r_P).

2.2. White LEDs

As described above, the light emitted by LEDs is generated in the active region of the LED junction. Up to now there is no element known which can be included in the junction to emit white light directly in an efficient way. Therefore, white light LEDs are produced using colour mixing. Possible mixing approaches are dichromatic, trichromatic or tetrachromatic approaches [59]. In these approaches single- and multiple-chip systems can be used to create the following colour mixes:

- blue and yellow light
- blue, green and red light
- blue, cyan, green and red light

In multi-chip systems, the light of various solid state light sources is mixed by a lens. For example, one red LED, one green LED and one blue LED are placed underneath a lens which mixes the colours to white (trichromatic system). These systems are sensitive to temperature changes and can have a small Colour Rendering Index (CRI) [60] and low chromatic stability [61] which is related to the temperature sensitivity. The single chip systems are based on two procedures:

- White light chip
- White light with wavelength conversion material

2.2.1. Colour Mixing

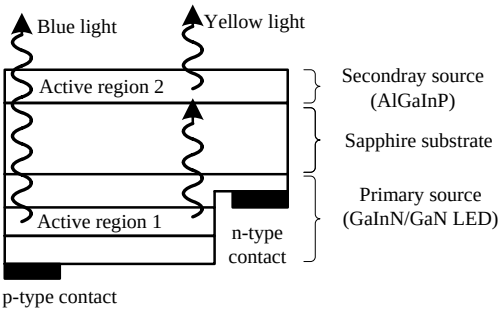


Figure 2.3: Schematic structure of a photon-recycling semiconductor LED [59]

The white light chip is based on a chip embedded with two active regions, the so called Photon-recycling Semiconductor LED (PRS-LED). The structure is shown in Fig. 2.3. As the figure indicates, the light emitted by the Gallium Indium Nitride (GaInN) LED is absorbed by the second Aluminium Gallium Indium Phosphide (AlGaInP) active region and re-emitted as lower-energy photons [59]. X. Guo et al. [62] implemented a new white light emitting diode using the structure shown in Fig. 2.3.

2.2.2. Luminescent Lighting

The wavelength conversion LED uses a single active region emitting single colour light. A part of this light is absorbed by a colour conversion material, i.e. silicon phosphor, which emits another light colour. This subsequent colour mix will result in a white light appearance. Several conversion methods are available, the most common ones are the following [63]:

- blue LED and yellow Phosphor
- blue LED and several Phosphors
- ultraviolet LED with Red, Green and Blue (RGB) Phosphors
- blue LED and Quantum Dot

Table 2.1 compares the different types of white LED lights. The present work focuses on white HP-LED lights of type one (blue LED and yellow Phosphor) of the single-chip approach based on wavelength conversion method. Since the invention of the blue LED, white LED lights have continued evolving. More than a decade ago, they are supplied by currents up

Table 2.1: Comparison of the different kinds of white light LEDs

Method	LEDs	Advantages	Disadvantages
Two or more colour LED chips	Combinations of LED chips (dichromatic, trichromatic or tetrachromatic)	Broad colour spectrum [60]	Temperature sensitive colours, bad stability, variable CRI Complex and dedicated electronic control for each colour needed [60]
Two or more active regions in a single LED chip	Combinations of semiconductors	High luminous efficacy [62, 64]	Low CRI [62]
wavelength conversion	Blue LED and yellow Phosphor	Relative low cost and most mature technology [65] Good CRI [60] High luminous flux [65]	Various colour temperatures range [60]
	Blue LED and several Phosphor	Broad wavelength spectrum [60] High colour quality [60]	Expensive [63]
	Ultraviolet LED with RGB Phosphors	Broad wavelength spectrum [63]	
	Blue LED and Quantum Dots	Similar spectrum to the Ultraviolet type [63]	

to tens of mA, small size (about 300 µm) and had an efficacy of 10 lm W^{-1} [66]. Through the years, the technology evolved until becoming competitive, in 2010 the efficiency was around 100 lm W^{-1} and the size increased to a millimetre square or more [66]. Still the price of LED lights

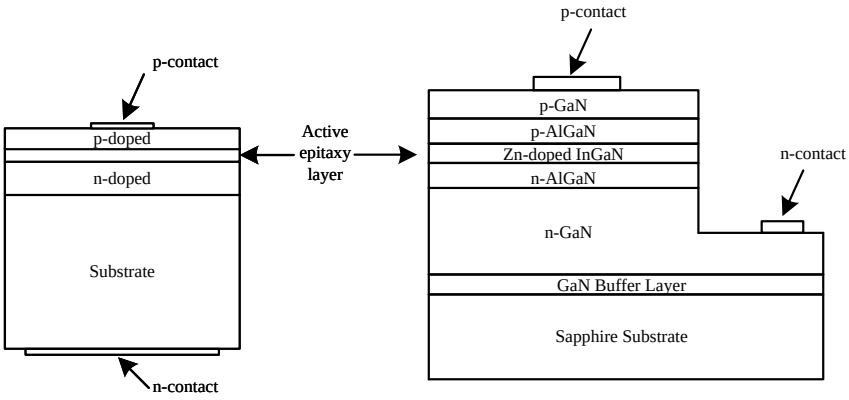


Figure 2.4: Basic LED chip structure with contacts and active region [68] (left) and structure of a blue LED based in InGaN/AlGaN heterojunction based on [69] (right)

is high compared to incandescent light bulbs, which makes it hard to conquer the market. However, the price of LED lights continues to decrease. Moreover, due to its lower power consumption and longer lifetime characteristics white LED lights are preferred wherever it is complex to replace a burned-out lamp as in the high ceilings of Buckingham Palace [66]. The longer lifetime and the lower power consumption are translated in a reduction of operational costs and have made white LED lights to be considered a green technology [67]. Since 2009, the approach of white LED lights using blue LED and yellow phosphor was predicted to dominate the market [60] and because of their advantages they have become the preferred choice for manufacturers and consumers.

2.3. LED Structure

Blue LEDs were the basis for white light generation and they have been a subject of research for decades. From the first LEDs using Silicon Carbide (SiC) films in the mid 1960s with very poor efficiency to 1994 where Isamu Akasaki, Hiroshi Amano and Shuji Nakamura invented an efficient blue LED for which they were awarded the Nobel Price in Physics in 2014, the LED efficiency improved from 0.03 % to 35 % [63, 67]. Current blue light LEDs can consist of following materials:

- Gallium Nitrate (GaN) with Aluminium Gallium Nitrate (AlGaN) quantum barrier
- InGaN
- Sapphire (Al_2O_3) as substrate
- Silicon (Si) as substrate

- SiC as substrate
- Zinc Selenide (ZnSe)
- Aluminium Nitride (AlN)

The initial blue LED structure proposed by Nakamura et al. [69] is shown in Figure 2.4 (left). Nowadays, different semiconductor structures are used. The most common materials are InGaN and GaN with various possible substrates (Si, SiC, Al_2O_3). The basic structure of an LED is shown in Figure 2.4 (right). It consists of an active layer, a p-doped material, an n-doped material as well as the substrate. The LED structure has evolved from a simple heterostructure model with bulk layer proposed by Nakamura et al. [69] to a structure with enhancements as Multiple Quantum Well (MQW), use of Quantum Dot (QD) varied quantum barriers, flip chip technology etc. Many of these enhancements have been developed to minimise the impact of the Droop effect, which is an effect describing an efficiency decrease when the forward current increases [70].

2.3.1. Active Region

The active region is the area of the LED where the light is created. It was discovered, that a variation of the MQW can improve the quantum efficiency. For example, OSRAM has patented an optical semiconductor device comprising an MQW structure shown in Figure 2.5. The active region is composed of the elements 6a, 6b, and 6c; where the QWs are the layers 6a and 6b. The layer 7 is used as an electron barrier and layer 5 is described as an n-buffer. The patent states that the emitting layer 6c is on top of the MQW 6a (GaInN)-6b (GaN). The thickness of 6a is less than 3 nm and for 6b is ≥ 3 nm. The indium content is preferably below 20 % and the x letter stands for the number of times the MQW is repeated (x=3 proposed in the patent). The MQW can be doped with silicon at a concentration of 10^{17} cm^3 to 10^{18} cm^3, which provides significant improvement compared to an undoped structure according to the patent [71]. Another improvement described in the patent is the stepped well layer 6a (60a to 63a) shown in Figure 2.6. Compared with the non-stepped well layer (right side of Figure 2.6) the stepped layer have an increased quantum efficiency, which is according to the authors due to the improved nucleation of InGaN-rich phases for the influence of the last single layer (63a) over the strain [71]. Another patent related to LEDs owned by CREE® consists of a double heterostructure for a blue LED with a p-layer of AlGaN, an n-layer of AlGaN and the n-type layer of GaN between the AlGaN layers. This patent highlights the advantages of a heterostructure compared to a homostructure, which can include enhanced emission, more efficient carrier confinement and a brighter output [72].

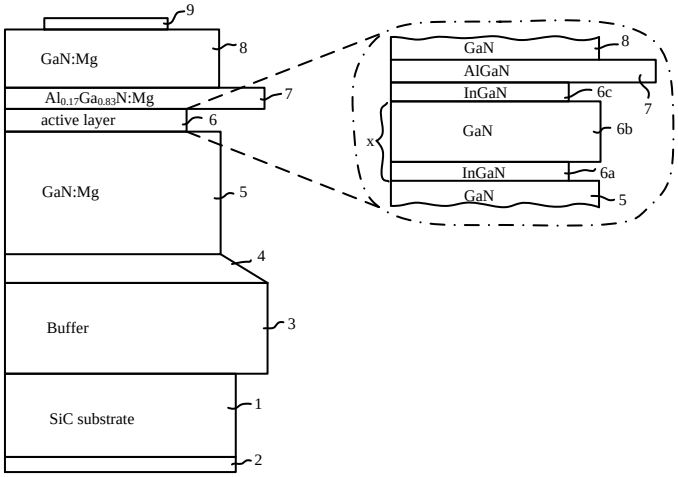


Figure 2.5: OSRAM patent of an optical semiconductor with MQW [71]

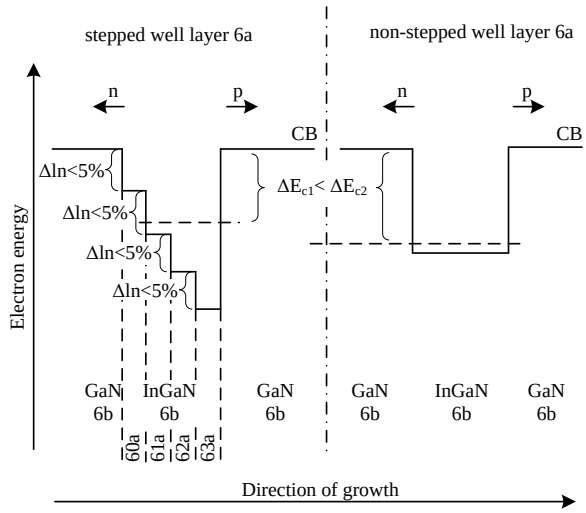
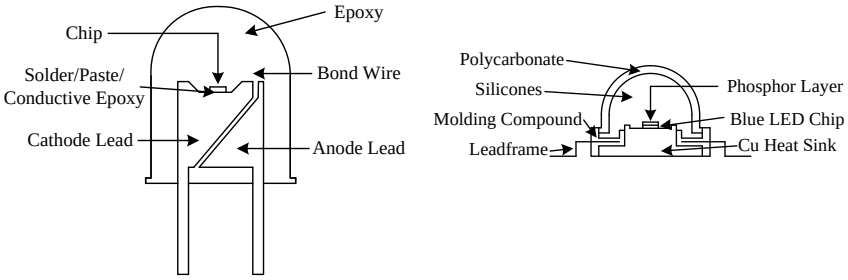


Figure 2.6: Stepped well layer of the OSRAM patent [71]

2.3.2. Dome

The dome is the top part of the LED. It is responsible to pass through the light and protect the silicon from the environment. Furthermore, the phosphor is embedded into the dome. It could also be used as a lens to change the light beam behaviour. The optical structures can define different per-



(a) (b)

Figure 2.7: Schematic of low power LED packaging (a) and of high power LED packaging (b) [73]

formances for the same blue LED chip. For example, OSRAM has two different lines for its high power LEDs the DRAGON and OSLON products are based on the same technology called ThinGaN [68]. The difference between these products is the target application. The golden DRAGON meets the requirements for wide angle light and standard PCB layout; for directed light, colour mixing or clustering the OSLON is the best option.

2.3.3. Package

LED packaging started with the invention of red LEDs. These LEDs were mostly used for indication due to their low luminance and supply energy lower than 0.1 W. The invention of the blue LED allows the creation of white light by conventing blue light into yellow light using a colour conversion material. This enables the usage LEDs for lighting applications, the size of LED chip rises and subsequently high power LEDs with an input current above 100 mA were born. High power LED packages are usually used for LEDs with a power above 1 W and a size larger than 1 m × 1 m [73]. The schematic design of a low power LED package is shown in Figure 2.7a. Compared to HP-LEDs, low power LEDs have no serious problems in heat dissipation. Since the invention of the HP-LED, the heat dissipation became a problem. The higher supply power leads to higher losses and to higher temperatures within the LED. If the heat is not conducted to the environment, the LED will overheat. In 1988, Luminleds proposed the leadframe plastics package structure (Luxeon) which is shown in Figure 2.7b. The LED chip is soldered to a large-size metal heat core consisting of copper which rapidly transports the heat to the LED mount. The chip is bonded with gold wires to reduce the bond-wire resistance. Current HP-LEDs supplied with a power up to 100 W have a package with a ceramic substrate

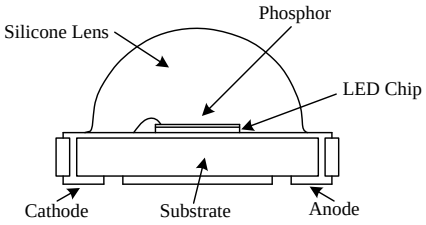


Figure 2.8: Cross-section of high-power LED lamp (CREE® XLamp®) [74]

or have a PCB as base i.e. CREE® XLamp® or Lumileds Rebel-series. The CREE® XLamp® cross-section is shown in Figure 2.8. All in all, the thermal resistance between LED chip and the environment is excessively reduced. [73]

2.4. LED Temperature

As soon as an LED is supplied with a current, visible light is generated and the junction temperature rises. Especially HP-LEDs, which are mounted on a cooling plate, are not 100 % efficient and have losses which result in a temperature increase. For example Cree® Xlamp® has an efficiency of 40 % implicating that 50 % to 60 % of the supply power is tuned into heat. LEDs are highly sensitive to the LED junction temperature. HP-LEDs operate at high temperature ranges of 50 °C to 150 °C at which their photometric, radiametric and colourimetric values differ significantly from their values at room temperature. Exceeding the maximum junction temperature of typicality 150 °C can cause permanent and/or catastrophic damage to the LED. Therefore, it is a must to know the LED junction temperature to enable constant light quality as well as long LED lifetime [75]. Current LED temperature determination strategies measure the system case temperature, pin temperature, board temperature, solder-point temperature or heat sink temperature. A physical model of the LED is used to calculate the junction temperature. Even tough, the measurement results cannot be compared between different LEDs, there is always an unknown thermal resistance between junction and the temperature sensor [76]. The International Commission on Illumination wanted to close this gap and introduced the CIE 225:2017 [76] in 2017. It describes how to measure or determine the junction temperature in an appropriate way. The LED junction temperature is a performance indicator for the thermal design. Furthermore, it plays a major role in lighting design. In the following text current junction temperature determination methods are described.

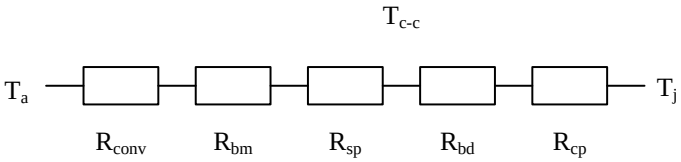


Figure 2.9: Thermal resistance model of a present LED [79, 80]

2.4.1. Temperature Measurement

Several methods for temperature measurement or temperature estimation have been discussed in the last decade. The conventional method is based on an external temperature measurement and uses a complex physical model of the LED structure to determine the junction temperature. Other approaches are the emission peak energy shift method [77], the radian energy method [78], the high energy slope method as well as the forward-voltage method [77]. The forward voltage method has been identified as the most accurate method with lowest complexity [77]. Therefore, this subsection discusses conventional methods and the forward voltage method.

Conventional

The conventional temperature determination is based on an external temperature measurement. The measured temperature is used to calculate the junction temperature of the LED. The thermal path between the temperature measure point, the junction and the calculation can be described as a simple resistor network. For an LED with an attached heat sink the network is shown in Figure 2.9. Where T_j is the LED junction temperature, T_{c-c} is the temperature at the LED solder point on the PCB and T_a is the ambient temperature. R_{cp} is the thermal resistance of the packaging of the HP-LED and is related to the package type of the LED, R_{bd} is the thermal bonding resistance between the LED substrate and the aluminium base which is determined by the bonding material and thickness, R_{sp} is the thermal spread resistance between the LED substrate and the aluminium base which changes with the size of the LED, R_{bm} is the thermal resistance of the heat sink and R_{conv} is the thermal convection resistance between the heat sink and the environment. A common equation to calculate the junction temperature of a semiconductor is (2.10) [28]:

$$T_j = R_{thJA}\, P_D + T_a \tag{2.10}$$

Where R_{thJA} is the thermal resistance between the junction and the ambient, P_D is the power dissipated by the LED and T_a is the ambient temperature. The problem arises in the calculation of the thermal resistance

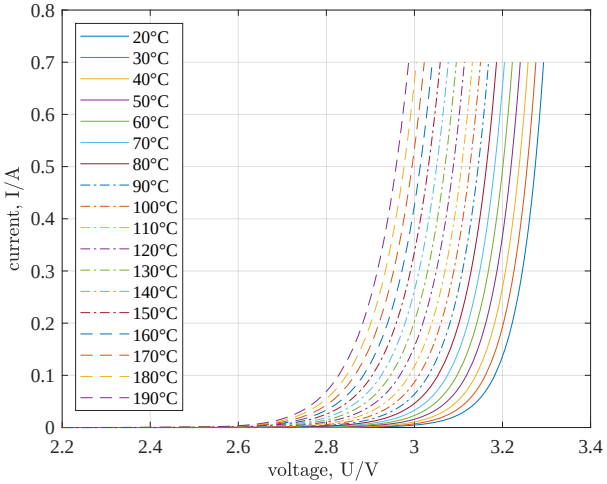


Figure 2.10: Characteristic curves of a blue GaN/InGaN-LED at different temperatures

between the junction and the ambient. The resistance is affected by different internal and external factors and boundary conditions of the LED. Complex studies and tools are usually required to find the correct parameter. Furthermore, the determination of the external temperature is complex. The best results can be achieved by using an insulated thermocouple with a good mechanic contact with the LED temperature point using thermally conductive epoxy or solder past. The amount of direct light exposed on the couple should be minimised [80].

Forward Voltage

To characterise the thermal performance of an LED, Acharya and Vyavahare [78] analysed the LED characteristics based on the forward current equation and the characteristic curves for different temperatures. The results of the current-voltage curves (Figure 2.10) show that the bias voltage decreases for higher temperatures with constant current. A linear variation for these curves at temperatures higher than 220 K can also be observed [78]. Some methods for junction temperature determination are based on the emission peak energy shift where the shift of the peak wavelength of the emitted light gives information about the temperature of the active region [77]. This is similar to the radian energy method discussed by Gu and Narendran [28] where the relative output of the LED depends on the temperature. Another method, the high energy slope method, uses the slope of the emission energy compared to the emission intensity to determine the temperature. The last method is the forward-voltage method which uses

the linear relation between forward voltage and temperature at constants currents [77]. Xi et al. [77] concluded that the forward-voltage method is the most accurate one giving an error range of ±3 °C. A variation of the forward voltage method is used by Moolman et al. [81]. They developed an equation based on the results of the calibration phase in which the forward voltage is defined in terms of the derivative respect to the temperature as follows:

$$V_f = A_0|_{I_f}\, T_j + V_0|_{I_f} \tag{2.11}$$

The work presents a relation between A_0 and V_0 for I_f, where A_0 is the derivative, V_0 is the voltage at T_j junction temperature of 0 °C in (2.11). Values of A_0 and V_0 can be used to calculate the junction temperature as a function of V_f for constant currents (2.12). The graphical realisation is shown in Figure 2.11.

$$T_j = A_0|_{I_f}\, V_f + T_0|_{I_f} \tag{2.12}$$

Roscam Abbing [21] collected several sensing methods of junction temperature from which the simplest one is ”two temperature calibration technique with current bias”. This method is based on the following equation:

$$T_j = \alpha + \beta V_f|_{I_D} \tag{2.13}$$

The constants α and β are calculated using two voltages by varying temperatures at a constant current I_D. The disadvantage of this approach is that it is related to a fixed current. The values of the constants have to be recalculated for different currents. Another method introduced by Roscam Abbing [21] is based on the relation of temperature and forward current, however, these require logarithm operations that increase the calculation costs. The complexity of this kind of operation implies more complex controllers. A similar method is proposed by Ke et al. [82] which improved the working conditions and considering resistive losses caused by the shift of the forward current for different temperatures. The authors define the equation of forward voltage as follows:

$$V_f = -AT_j + B + R_s\left(I_{F1} - I_f\right) \tag{2.14}$$

V_f and I_{f1} are values of a calibration experiment and R_s is the resistance of the LED. The value of R_s is obtained as the slope of the forward current at different ambient temperatures. The accuracy of this method is in a range of 3 °C to 10 °C for an experiment based on a calibration with 130 mA. The literature research led to the conclusion that less complex and more accurate methods to calculate the junction temperature are based on the forward voltage. This method can be implemented with some vari-

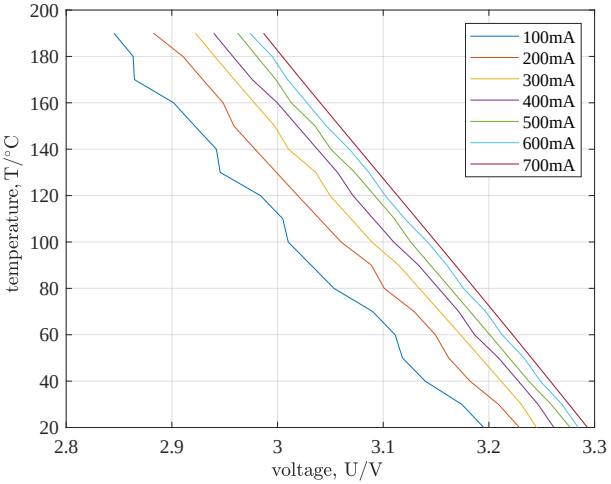


Figure 2.11: Voltage temperature relation at constant currents showing the mainly linear relation

ations in order to improve its generalisation and accuracy. Despite the developed methods for the calculation of the junction temperature, their implementation into controllers is considered to be too complex and only realisable when supported by specialized instruments. Furthermore, the mentioned methods do not allow a temperature determination at different currents. Consequently, the forward voltage is calibrated and analysed for a HP-LED.

2.4.2. Calibration

The coefficients A_0 and T_0 (2.12) have to be calibrated for each single LED. According to Ke et al. [82], Ye et al. [83] the calibration can be performed by supplying the LED for a very short time, i.e. $<100\,\mu s$, to avoid self-heating. Special thermal conditions and timings have to be met for pulsed LED measurement. Thermal effects for pulsed LEDs are analysed by Zong et al. [76], Miller et al. [84] for different application areas. Miller et al. [84] describes experimental results of a thermal analyses for pulsed LEDs, where the CIE225:2017 Zong et al. [76] is mainly addressing optical measurement of HP-LEDs. These optical measurements are difficult, since LEDs are very sensitive particularly at high temperatures. Especially the junction temperature is a significant condition for the optical measurement. LED manufacturers often measure the LED characteristics using millisecond or microsecond long pulses, assuming that the junction temperature stays at room temperature (typically 25 °C). There-

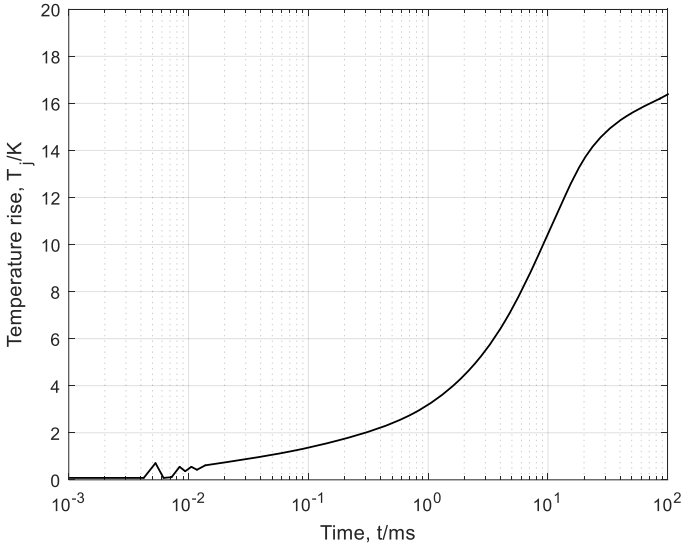
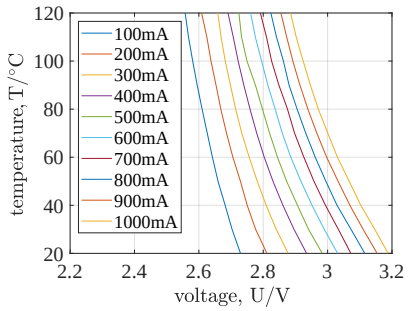
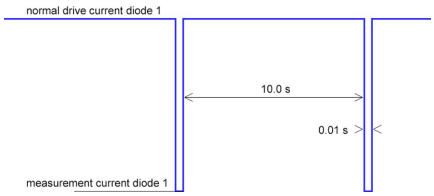


Figure 2.12: Junction temperature rise, ΔT_j of a 1 W HP-LED attached to a TCM from 0 ms to 100 ms showing a temperature rise of 3.7 K within 1 ms [76]

fore, published HP-LED specification normally refer to a junction temperature of 25 °C. As already mentioned, HP-LEDs used in lighting applications are commonly operated in DC mode with a junction temperature of 50 °C to 120 °C. The CIE225:2017 [76] addresses thermal specifications of pulsed measurement for HP-LEDs to provide information on HP-LEDs in standard operation conditions [76]. Furthermore, Thermal Transient Effect (TTE) will occur if the measurement time is too short [83, 85–87]. Figure 2.12 gives information about the rapid junction temperature rise of an 1 W HP-LED. It can be identified that the forward voltage and the current has to be measured before the junction temperature rises in this case 10 µs after supplying the LED. To achieve short current pulses with a current of up to 1 A, a calibration system is developed. It is based on a 1 A constant current controller CAT4101 from ON Semiconductor. It provides a current pulse of maximum 1 A for a minimum pulse time of 5 µs. The pulse input trigger of the current controller is driven by an SMT32 microcontroller in such a way that current pulses with a length of 20 µs are generated when a button is pressed. The current provided by the chip can be adjusted by a potentiometer. The board layout as well as the schematic of the calibration PCB are shown in Appendix A in Figure A.1 and Figure A.2 respectively. Figure A.3 shows a picture of the assembled calibration PCB. The constant ambient temperature of the LED is realised by using a TEC-Mount from Arroyo (Arroyo Instrument 5305) allowing to adjust



(a)



(b)

Figure 2.13: Result of the calibration for currents of 100 mA to 1000 mA with an increment of 100 mA (a), junction temperature measurement technique for a practical setup conducted at normal drive current and measured every 10 s by lowering the drive current for about 10 ms [89] (b)

the temperature of a device fixed on a mount. Fig 2.13a depicts the results, i.e. temperatures with respect to voltages at different currents, using a Cree® XPLAWT White HP-LED a type of XLamp®. For lower currents such as 100 mA or 200 mA, the function can be described as nearly linear. At higher currents especially at 1 A the function is getting more and more quadratic. A reason for this effect is explained by Gacio et al. [26]: the LED resistance changes with temperature. To overcome this effect, three variations of the method are identified. The first approach is to linearise the forward voltage in the operation point of the LED at different temperatures. Two parameters are needed for each current at which the temperature has to be identified. This results in 20 values for the example shown in Fig 2.13a. One multiplier and one addition is needed for the calculation of the temperature (2.12). Given data from the CREE® datasheet [88] and a test with an LED mounted on a cooling plate provide information about the operation temperature for different currents. The second approach is to use a quadratic function for the description of the temperature voltage relation. This allows to determine the temperature of the LED in all operation points covered by Fig 2.13a. Disadvantage of this approach is the moderate increase of the complexity of the temperature calculation. Three constants for each current are necessary in this approach, which results in a total of 30 parameters. Three multipliers and two additions are needed for the related temperature calculation (2.15).

$$T_j = A_1|_{I_f} V_f^2 + A_0|_{I_f} V_f + T_0|_{I_f} \tag{2.15}$$

The third approach is the Pulsed Junction Temperature Measurement (PJTM)

introduced by Ye et al. [83], Keppens et al. [89]. This measurement technique reduces the LED forward current to a low current of 100 mA or 200 mA for a short period of time. Due to the linearity of the temperature, voltage relation at low currents the linearised function can be used. A further advantage is that only two coefficients are needed to determine the LED temperature, subsequently the calibration can be reduced to one constant current measuring the forward voltage at different temperatures. Disadvantages of this technique are the more complex current controller and the pulsed current which can result in TTE. A supply current versus time diagram is shown in Fig 2.13b, the supply current is kept constant for 10 s. In this period the LED is used as a light source. Afterwards, the current is reduced for 10 ms. In this time the temperature of the LED is determined. The measurement current is low, in this phase almost no amount of light is generated by the LED. Cain et al. [90] mention, that the time needed by the controller to reduce the current will cool down the LED and impair the measurement results. Furthermore, circuit transients occur directly after switching the current from high current to low, which can result in a measurement error, too. This is why only a short period of time can be used to determine the LED temperature. And even then, a contention factor has to be used to correct the cooling effect by the small current. To validate the methods linear, quadratic and PJTM, the coefficient of determination (R^2) is calculated [91]. The R^2 allows to qualify a linear regression statistically, it can be calculated by (2.16).

$$R^2 = \frac{SS_{between}}{SS_{total}} = 1 - \frac{SS_{error}}{SS_{total}} \tag{2.16}$$

$$SS_{total} = \sum (y - \bar{y})^2 \tag{2.17}$$

The variation that has been explained by the model is the difference between the total sum of squares and the residual sum of squares and is called the between groups sum of squares or the regression sum of squares ($SS_{between}$ or $SS_{regression}$) [92]. SS_{total} is calculated by the sum of squared deviations from the mean ($\bar{y}$). The problem that arises when using the R^2 is that the more values are used, the better the R^2 value gets. If enough values are used for the R^2 definition, an R^2 can get equal 1. To overcome this fact, the adjusted R^2 was introduced, it can be calculated by (2.18)

$$R^2 = 1 - \frac{n-1}{n-p}\frac{SS_{error}}{SS_{total}} \tag{2.18}$$

Where n is the number of observation, p is the number of the regression coefficient. It has to be noted that p includes the intercept, for a linear fit p is 2. As the standard R^2 is highly dependent on the number of used points, the adjusted R^2 values are used to evaluate the approximations.

Table 2.2: Adjusted R^2 values for three evaluated temperature estimation methods

Current	Adjusted R^2 Linear	Quadratic	PJTM
100 mA	0.9845	0.9997	0.9845
200 mA	0.9791	0.9995	0.9791
300 mA	0.9664	0.9976	-
400 mA	0.9732	0.9994	-
500 mA	0.9765	0.997	-
600 mA	0.9747	0.9991	-
700 mA	0.9794	0.9989	-
800 mA	0.9759	0.9989	-
900 mA	0.9778	0.9986	-
1000 mA	0.9798	0.9988	-

R^2 values for the linear and quadratic approach are listed in Table 2.2. Since, the PJTM is based on one specific current already used in the linear method, the R^2 for the linear fit of 100 mA and 200 mA and PJTM are the same. Table 2.2 shows that the quadratic approximation has the slightest error. With an $R^2 \approx 0.99$ the fit is quite well. For the linear fit the lower currents, which are used in the PJTM fit best. The higher the current gets, the worse the approximation fits, this is exactly what was identified earlier in the chapter. When R^2 is built up in the standard operation region of the LED, it will get higher.

2.5. Multiphysic Simulations

To identify thermal hotspots in the LED structure as well as in the dome and package, a multiphysic simulation is performed. LED simulations are complex due to the complex desired structure. It is difficult to choose the right model parameter and define the geometry as well as the material type. The simulation can be time consuming because of the complex structures which differ from sicknesses such as 2 µm to 1 cm. Different simulation tools are available on the market which provide the physics to simulate LEDs, especially APSYS from Crosslight, SiLENSe from STR Group, ATLAS from SILVACO and COMSOL multiphysics. In this work ANSYS was used to simulate the active region because of the better implemented semiconductor lighting library. The entire LED is simulated by the simulation tool COMSOL multiphysics which allows to simulate a Three-Dimensional (3D) structure with a variation of physical behaviours.

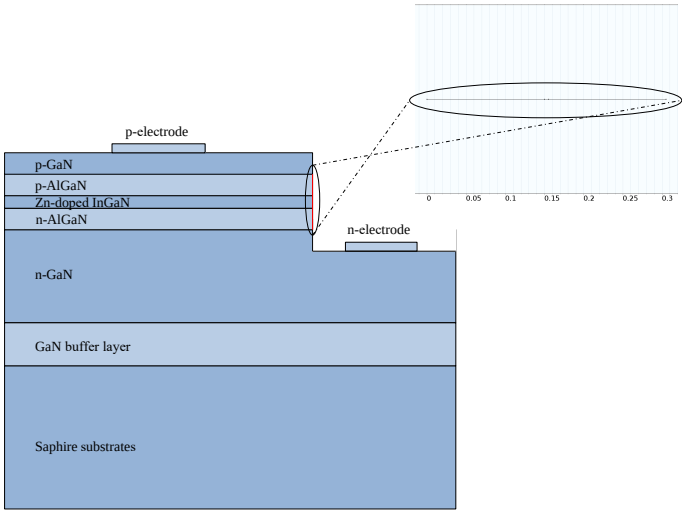


Figure 2.14: Semiconductor structure of a blue LED with double heterostructure InGaN/AlGaN by [69]

2.5.1. LED Semiconductor Structure

First of all, in COMSOL the LED structure has to be modelled. The shown structure is a double heterostructure InGaN/AlGan by Nakamura et al. [69]. For the simulation, only the active region of the LED is simulated. It has a sandwich structure consisting of 50 nm $In_{0.06}Ga_{0.94}N$ surrounded by a 150 nm layer of $Al_{0.15}Ga_{0.85}N$. The structure was reduced to an One-Dimensional (1D) model to speed up the simulation, see example in Fig. 2.14. The cross section of the active region is set to 200 µm × 200 µm which is a typical size. After simulating the basic structure using COMSOL, more complex structures of the active region were simulated with the APSYS software from Crosslight. It offers specific features for the LEDs. Compared to COMSOL, APSYS already integrates models for polarization, temperature dependence energy band-gaps and many more.

2.5.2. LED With Dome And Package

The Simulation of the LED with dome and package is performed for two different structures. The first structure is based on the work of Liu et al. [27]. The structure was adapted in such a way that a phosphor layer was included on top of the LED chip. Two variants of phosphor conversion are implemented, remote phosphor, where the phosphor is placed apart from the LED chip and proximate conformal phosphor where the phosphor is placed around the LED chip. The possible phosphor distributions

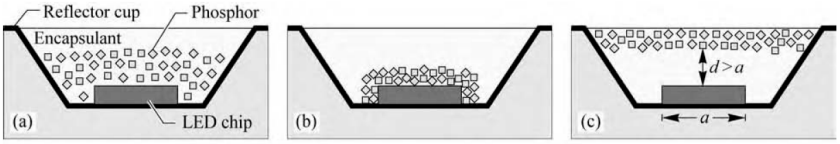


Figure 2.15: (a) Proximate phosphor distribution, (b) proximate conformal phosphor distribution, and (c) remote phosphor distribution in which phosphor and chip are separated at least one times the lateral dimension of the chip [59]

are shown in Figure 2.15. Heat is created in the phosphor layer by two mechanisms [34]. The first mechanism is pure absorption, the blue light energy is transformed into heat. The second mechanism is a transformation from blue light to yellow light. Due to collision losses heat is created, too. Both mechanisms can be added and substituted by a secondary heat source in the LED [34]. The total thermal power of the phosphor region can be written as (2.19)

$$Q_{ph} = P_{Bi} \cdot Abs \cdot \frac{v_B - \eta_{ph_q} v_Y}{v_B} = \int \dot{q}_{ph}\,(x, y, z)\, dV \tag{2.19}$$

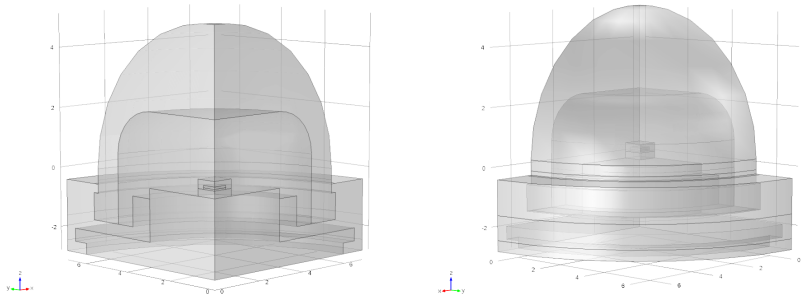
$$P_{Bi} = P_{LED} \cdot \eta_{LED} \tag{2.20}$$

where Abs is the absorbency of the phosphor region, v_B and v_Y are the effective blue and yellow photon frequencies, η_{ph_q} is the quantum conversion efficiency of the phosphor, $\dot{q}_{ph}$ is the thermal power density of the phosphor region [34]. The phosphor in the phosphor layer is not equally distributed [34]. Nevertheless, for an approximation the phosphor can be modelled in such a way that it creates heat by the loss factor of the phosphor, this considers the assumption of equally distributed heat source. The LED chip can be modelled as a uniform volume heat source [34]. The efficiency of a Cree® LED is noted in a rage of 50 % to 60 % [93]. An conservative thermal power estimation of 0.75 is also noted by Liu et al. [27]:

$$P_t = 0.75 \cdot V_f \cdot I_f \tag{2.21}$$

$$P_t = 0.75 \cdot P_{LED} \tag{2.22}$$

Where P_t is the thermal power, V_f is the forward voltage, I_f is the source current to the LED and P_{LED} is the source power of the LED. Optimally, 25 % of the LED supply power is converted into light. This light is only blue coloured. To achieve the desired white light output, a part of the blue light has to be shifted to yellow light using a colour conversion layer. The colour conversion layer consisting of phosphor in an encapsulate converts

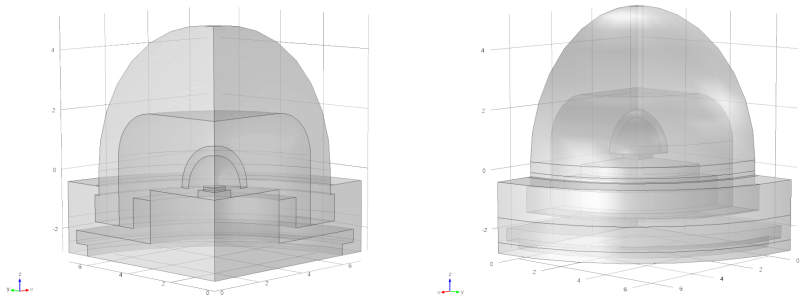


(a) (b)

Figure 2.16: One quarter of the 3D LED structure with proximate phosphor on top of the active region [27]

approximately 40 % [94] of the emitted blue light with an efficiency of 77 % to 90 % [95] into yellow light. The mixture of remaining blue and created yellow appears to be white colour. First simulations were performed based on the findings of Liu et al. [27]. Dimensions as well as material parameters where used as shown in Table 2.3. The remaining material parameters are taken from the COMSOL material library. Not defined sizes are determined from a real LED. Figure 2.16 depicts the resulting 3D geometry of the simulated LED. Considering the symmetry, the geometry of the LED is designed as a quarter of the original structure, it is mirrored on the zx-axes and the zy-axes which generates a model of the complete LED, however, it reduces the simulation effort. As the chip centre is square shaped a 2D axisymmetric simulation can not be performed. Figure 2.17 shows the same LED structure using the remote phosphor technology where phosphor is placed radial around the chip as shown in Figure 2.15 (c). With a power consumption of 1.18 W, this LED is a mid power LED. The heat generation power of the chip and the phosphor are calculated using the efficiency of the materials.

$$P_{tj} = P_{LED} \cdot (1 - \eta_s) \tag{2.23}$$
$$P_{tj} = 1.1804\,\mathrm{W} \cdot 0.75 \tag{2.24}$$
$$P_{tj} = 0.8853\,\mathrm{W} \tag{2.25}$$
$$P_{tp} = P_{LED} \cdot \eta_s \cdot \eta_p \cdot \left(1 - \eta_q\right) \tag{2.26}$$
$$P_{tp} = 1.1804\,\mathrm{W} \cdot 0.75 \cdot 0.4 \cdot 0.2 \tag{2.27}$$
$$P_{tp} = 0.071\,\mathrm{W} \tag{2.28}$$



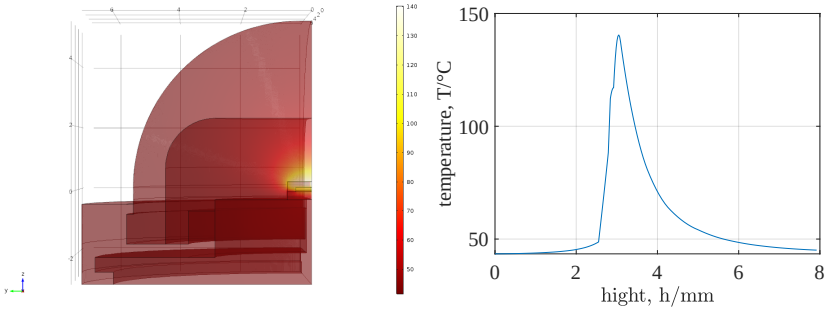
(a) (b)

Figure 2.17: One quarter of the 3D LED structure with remote phosphor placed in the silicon encapsulate [27]

Where P_{tj} is the thermal power of LED junction, η_s is the efficiency of the LED, η_p the phosphor light absorbing coefficient and η_q the phosphor efficiency. This values combined with the values of Table 2.3 result in a complete simulation environment. The stationary simulation with COMSOL was performed with an ambient temperature of 20 °C. The heat transfer coefficient to the heat sink was set to 1984 $\mathrm{W\,m^{-1}\,K^{-1}}$ and the surrounding air was set to5 $\mathrm{W\,m^{-1}\,K^{-1}}$. Results of the simulation are shown in Figure 2.18. The temperature distribution is shown in a 3D plot with a heat colour map (Figure 2.18b) and the centre temperature distribution of a 3D cut line in z direction (Figure 2.18b). Cut line results show the maximum heat in the LED structure in Figure 2.18 (b). The same result plots are shown for the remote technology in Figure 2.19. Maximum temperatures occur in the phosphor layer for both simulations remote phosphor and proximate conformal phosphor. Temperatures in the active region of the LED are equal in both simulations at approximately 114 °C to 115 °C. Compared to the proximate conformal phosphor of 137.5 °C, the phosphor temperature of the remote phosphor 135 °C is 2 °C lower. Despite worse thermal conductivity of the acrylic gas encapsulate, the larger area in which blue light is converted to yellow, reduces the power loss density of the phosphor layer. The simulation results are supported by results from Luo et al. [32], Kuo et al. [96], Liu et al. [97]. Therefore, the simulation environment as well as material parameters can be identified as applicable. The simulation geometry is now adapted to the LED type used in this work, the CREE® XLamp® XP-L High Intensity LED. To identify the sizes and the structures one LED was cut in the centre and placed under an electron microscope to get an image of the cross section of the LED. The resulting electron microscope image can be seen in Figure 2.20. Using

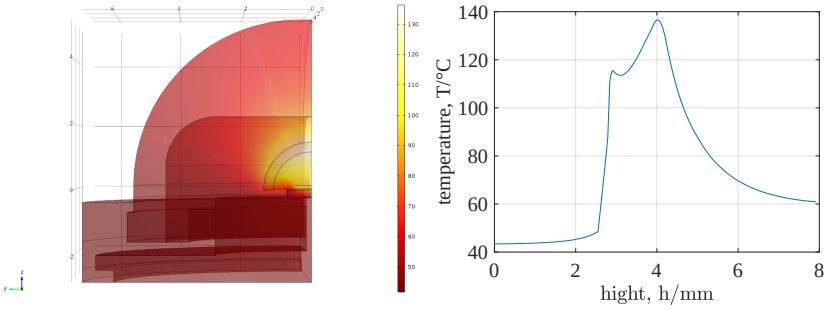
Table 2.3: Dimensions and thermal parameters of the LED module [27]

Component	Parameter	Symbols	Value	Unit
LED chip	length	-	0.96	mm
	width	-	0.96	mm
	thickness	-	0.08	mm
	thermal conductivity	-	40	W/(m K)
	LED input power	Q	1.1804	W
	light radiation power	Q_i	0.2951	W
	light generation rate	Q_h	0.8853	W
TIM	length	a	0.96	mm
	width	b	0.96	mm
	thickness	t_{TIM}	0.05	mm
aluminium stage	length	c	1.45	mm
	width	d	1.45	mm
	thickness	t_{alu}	0.24	mm
	thermal conductivity	k_{alu}	236	W/(m K)
copper heat sink	diameter of disc 1	D_1	2.91	mm
	diameter of disc 2	D_2	6.52	mm
	diameter of disc 3	D_3	5.97	mm
	thickness of disc 1	t_1	1.74	mm
	thickness of disc 2	t_2	0.44	mm
	thickness of disc 3	t_3	0.37	mm
	thermal conductivity	k_{cop}	393	W/(m K)



(a) (b)

Figure 2.18: 3D simulation result of proximate conformal phosphor structure(a) and the heat distribution in the centre(b)



(a) (b)

Figure 2.19: 3D simulation result of remote phosphor structure(a) and the heat distribution in the centre(b)

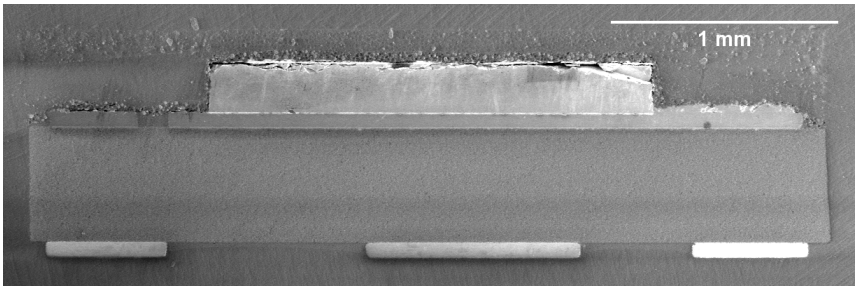


Figure 2.20: Cross section electron microscope image of the used CREE® XLamp® XP-L High Intensity LED with scale bar

the tool imageJ from NIH Image the sizes and thicknesses of each layer were identified and listed in Table 2.4. The REE® XLamp® XP-L High Intensity LED was designed as geometry in COMSOL using the identified values which allow a faithful reconstruction. The heat source of the active region is again designed as a heat source block corresponding to the results of the previously performed simulations. The energy converted by the phosphor to be heated is also modelled as a heat source block on top of the LED chip. In the electron microscope image, Figure 2.20, it can be seen that the whole LED is covered with a phosphor layer. This also applies for the region around the LED chip. To prevent yellow light output of this phosphor region, it is covered by a non-transparent white material. As a result of the coverage, only the phosphor placed on top of the active layer will produce heat and is also modelled by a heat source block. Material parameter have been taken from the datasheet [88]. The CREE® XLamp® XP-L is a high intensity LED with a supply power of 4.35 W [88], which

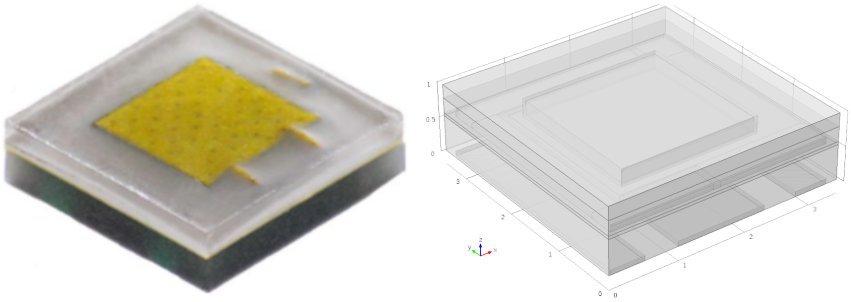
Table 2.4: Identified dimensions of the CREE® XLamp® XP-L High Intensity LED

Component	Parameter	Symbols	Value	Unit
LED dome	dome hight	-	0.19	mm
	white cover	-	0.42	µm
LED chip	length	-	3.45	mm
	width	-	3.45	mm
	thickness	-	223	µm
	LED input power	Q	4.35	W
	phosphor thickness	-	30	W
body	cooper hight	-	73	µm
	body hight	-	500	µm

results in following power:

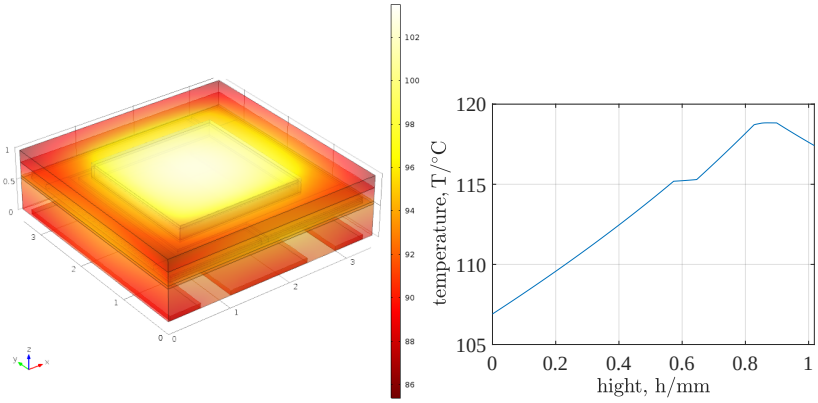
$$P_{tj} = P_{LED} \cdot (1 - \eta_s) \tag{2.29}$$
$$P_{tj} = 4.35\,\text{W} \cdot 0.75 \tag{2.30}$$
$$P_{tj} = 3.2625\,\text{W} \tag{2.31}$$
$$P_{tp} = P_{LED} \cdot \eta_s \cdot \eta_p \cdot \left(1 - \eta_q\right) \tag{2.32}$$
$$P_{tp} = 4.35\,\text{W} \cdot 0.75 \cdot 0.4 \cdot 0.2 \tag{2.33}$$
$$P_{tp} = 0.261\,\text{W} \tag{2.34}$$

The problem, which occurs here, is a higher thermal loss because of a smaller and compact geometry paired with a high supply power. To handle the higher thermal loss in the LED and allow a better heat flow to the heat sink, a third thermal connector is placed on the bottom of the LED to reduce the thermal resistance between the LED package and board. Furthermore, the thermal heat flow inside of the LED is enhanced by using materials with better thermal conductivity. A picture of the LED and the resulting simulation structure can be observed in Figure 2.21. The LED dome and the white light blockage structure consist of silica glass, the base structure has similar thermal conductivity like alumina, the active region material is gallium nitride, contacts consist of copper and the chip consists of silicon. The phosphor layer of the white light LED consists of cerium phosphide [28]. Gallium phosphide embedded in COMSOL material bibliography has similar thermal behaviour and is therefore used for the simulation. To verify the simulation of the LED, the simulation was initially performed with a stationary setup which will result in the maximum temperature occurring in the structure. The results show the temperature distribution in the centre of the LED from bottom to top in line with the previous simulations. This allows to recognise the differences in the temperature of the



(a) (b)

Figure 2.21: Picture of the used CREE® XLamp® XP-L [88] (a) and the geometry of the LED (b) build in COMSOL with sizes from table 2.4



(a) (b)

Figure 2.22: 3D simulation result of remote phosphor structure(a) and the heat distribution in the centre(b)

active region and the phosphor layer respectively. Results of this study are shown in Figure 2.22. Figure 2.22a shows the 3D geometry with a colour map, Figure 2.22b shows the thermal distribution in the centre of the LED similar to the simulations performed previously. To verify the simulation results and compare them to experimental measurements of the real LED the simulation was performed in a time dependent study. This study shows how the LED heats up from a defined start temperature. For the experimental measurement an IR-Camera is used, the InfraTec ImageIR 8380S uses an Indium Antimonide (InSb) focal plane array (FPA) snapshot detector with a geometric resolution of (640 × 512) pixel and a spectral

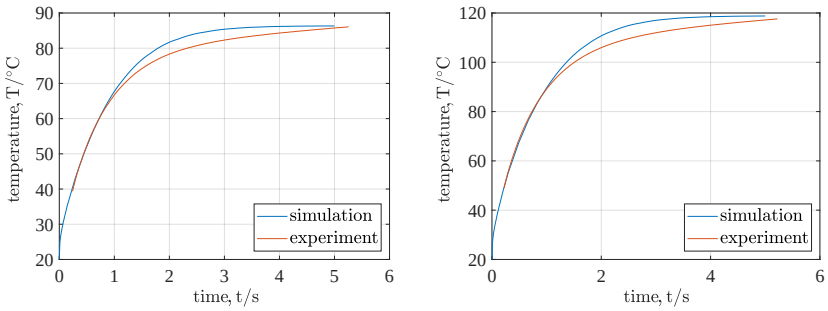


Figure 2.23: Simulation results compared to experiment results of the LED step response for a forward current of 0.7 A (a) and 1 A (b)

range of 2 µm to 5.7 µm. A comparison of the results with data from the IR-camera where the temperature is measured over time, can support the simulation results. The simulation and the experiment are performed for two different forward currents, 0.7 A and 1 A. In Figure 2.23a the results for the forward currents of 0.7 A is shown, the results for the forward currents of 1 A is shown in Figure 2.23b. A slight difference between simulation and experiment can be detected in Figure 2.23. The temperature of the experimentally determined LED temperature rises slower when the temperature of the LED increases. Reason for this behaviour is that the LED is supplied with a constant current and if the temperature of the LED increases, the forward voltage of the LED decreases (Figure 2.11). When the forward voltage decreases and the forward current is constant, the supply power of the LED decreases as well. In contrast to the experiment, the supply power in the simulation is constant, which characterises the deviation in Figure 2.23. Taking this fact into account, the measurements of the camera and the simulation results fit well, thus the results of the simulation can be seen as proofed. Analysing the results, it can be identified that the phosphor layer is only slightly hotter compared to the chip temperature. To check how this detail changes at different supply power levels, the simulations are executed again over the entire operation range. Temperatures of the chip as well as of the phosphor are shown in Table 2.5. The table can be used to clarify whether the forward voltage method can be used to determine the chip as well as the phosphor temperature.

2.6. Cooling Mechanisms

Cooling an LED reduces the thermal resistance between LED and environment and helps to reduce the internal temperature. Cooling can be separ-

Table 2.5: Temperature of the LED chip compared to the phosphor temperature at different supply power

LED power	temperature chip	temperature phosphor
0.0 W	20.00 °C	20.00 °C
0.5 W	31.36 °C	31.36 °C
1.0 W	42.72 °C	42.72 °C
1.5 W	54.08 °C	54.08 °C
2.0 W	65.43 °C	65.44 °C
2.5 W	76.79 °C	76.80 °C
3.0 W	88.15 °C	88.16 °C
3.5 W	99.51 °C	99.52 °C
4.0 W	110.87 °C	110.88 °C

ated into two main categories: passive cooling and active cooling. Both categories have their right to exist and are applied in different areas. This section will give an overview of passive and active cooling mechanisms and their scope of application. Furthermore, advantages and disadvantages of both categories are shown. Electrical powered devices such as LEDs dissipate heat to the ambient. (2.35) is the typical equation used to calculate the dissipation.

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{2.35}$$

Where θ_{JA} is the thermal resistance, T_J is the junction temperature, T_A is the ambient temperature and P_D is the thermal power dissipation. Rearrange (2.35) to (2.36) discovers the maximum power that can be dissipated.

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}} \tag{2.36}$$

θ_{JA} is in fact calculated out of at least two thermal resistances in series. The first is the thermal resistance inside the device package between the junction and the attachment position θ_{JC}. The second is the thermal resistance between the device compound and the ambient θ_{CA}. θ_{JC} is defined by the device architecture and therefore by the device manufacturer. θ_{CA} is the resistance which can be adapted by the cooling mechanisms. It can be divided into two θ_{CS} and θ_{SA}, θ_{CS} is the thermal resistance of the device's compound and the cooling mechanism and θ_{SA} is the thermal resistance

Table 2.6: Comparison of heat sink thermal resistances

standard	additively	unconstrained
0.301 °C W^{-1}	0.243 °C W^{-1}	0.231 °C W^{-1}

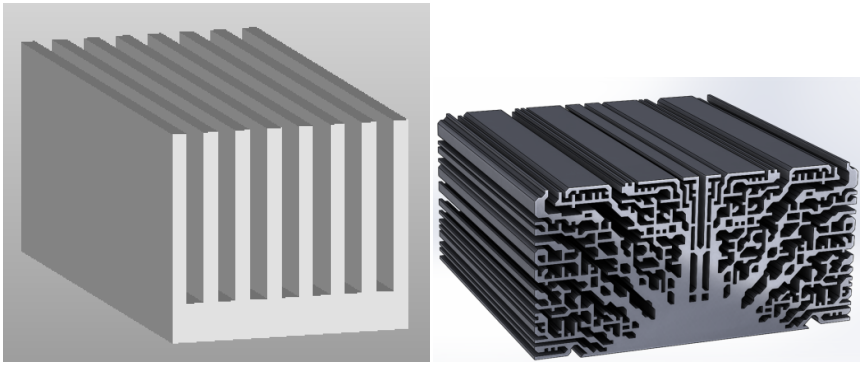
between cooling mechanism and ambient.

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \tag{2.37}$$

θ_{JC} and T_{JMAX} are given in the data-sheet of the devices. Passive and active cooling mechanisms can effect the thermal resistance θ_{SA} in various intensities [98].

2.6.1. Passive Cooling Mechanisms

Passive cooling mechanisms are based on a structure with a low thermal resistance and a hight surface area to reduce θ_{SA}, i.e. a heat sink. The higher the surface of the heat sink, the lower the thermal resistance θ_{SA} to the ambient. Figure 2.24a shows a typical heat sink used in typical applications. Using thin fines, a structure with a high surface area and a simply geometry can be created. This kind of heat sinks is benchmarked with respect to its ability to dissipate heat for a given ambient air speed. COMSOL [99] shows a method to evaluate this curve and to test the dissipation of heat sinks in a rectangular channel with inlet and outlet. The performance of a heat sink is given as the thermal resistance to the ambient. The lower the resistance, the better the heat sink performance. To increase the heat sink performance and the cooling property, the structure has to be optimised. Bornoff and Parry [100] gives an example using constructal law and evolutionary structural optimisation. The design starts with the definition of the size of the baseplate and the maximum size of the overall heat sink. By using additively design growth and a subsequent growth stage consisting of three growth periods, a minimum thermal resistance can be achieved. Figure 2.24b shows the result of the optimisation. Compared to a standard heat sink with upright big fins (standard in Table 2.6), the additively designed heat sink improves the thermal resistance by 20 %. An unconstrained heat sink growth is achieved by a heat sink with upright small fins and results in a even better thermal resistance with an improvement of 23 % (2.6). The outcome of this study is that the thermal resistance of a heat sink cannot be reduced beneath the minimum thermal resistance of a heat sink with small fins. To increase the heat dissipation of the cooling mechanism, an active retraced airflow is necessary.



(a) (b)

Figure 2.24: Picture of a typical heat sink (a) and a new heat sink design using constructal law and evolutionary structural optimisation (b) [100]

2.6.2. Active Cooling Mechanisms

Active cooling is often based on passive cooling, the difference is that an airflow is created to enhance the heat flux to the environmental air. The airflow can be created in several different ways, e.g. by a fan. In the last decades new approaches were developed to create airflow without using radial motor turning of a fan. The basic idea is to reduce the amount of moving elements and bearings to reduce abrasion and sources of defects. Furthermore, in most cases a fan is noisy and disturbing. That is why silent or noiseless active cooling is becoming more popular and thus research interest increases. New approaches comprise ionic winds, where an airflow is created by ions emitted by an electrode and synthetic jets where small air jets are created to reduce the thermal resistance of the heat sink to the ambient θ_{SA}.

Ionic wind

Ionic winds are used similar to the wind created by a fan. An airflow is generated pointing on a heat sink to create convection and to reduce the thermal resistance. An ionic wind generator consists of an emitting electrode and a collector [101]. The electrode can have various shapes, e.g. needle tip, ball or long flat. Whereby different electrode shapes will change the electric field and therefore also change the generated wind stream. In basic systems the collector consists of an electric conductive mesh, which creates a high collector area and allows airflow through the collector. The design of the collector will change the shape of the electric filed respectively. Collector and emitter facing each other. By applying a high-voltage difference on the emitter and collector, an electric field is cre-

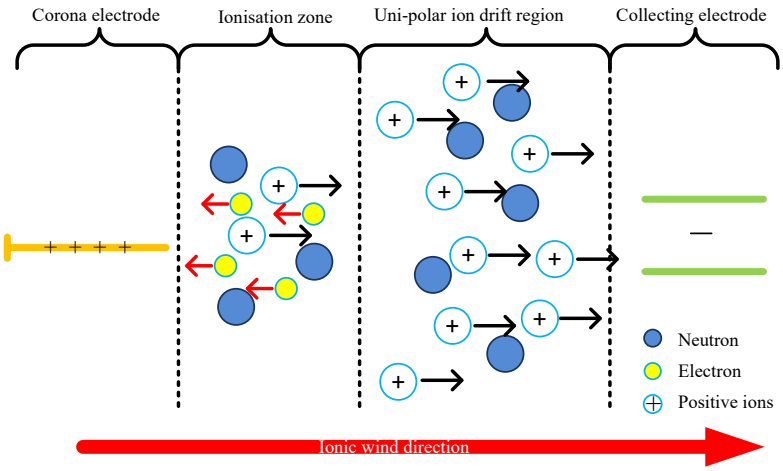


Figure 2.25: Principle of ionic wind generation showing electrode, cathode and the region where airflow is created [101]

ated. If the voltage exceeds a certain value, the corona inception voltage, a discharge occurs. The voltage depends on the geometrical structure, the distance between emitter and collector and the materials of both. Ionic winds will occur in a voltage range of 4 kV to 12 kV which is between the corona inception voltage and the spark over voltage where an electric arc is generated and the air gets electrically conductive. Ionic winds are generated at rather small currents of few µA resulting in a small power consumption [102, 103]. Between emitter and collector two regions can be identified where airflow is created: the ionisation zone and the uni-polar ion drift region as illustrated in Figure 2.25. Inside the ionisation zone, ions and electrons are generated by corona discharge. The positively charged ions are attracted by the collector and move into the uni-polar ion drift region, whereby the electrons are attracted by the emitter. Inside the uni-polar drift region, the positive charged electrons collide with air molecules and transfer the coulomb force to the air molecules. Air molecules are accelerated in the direction of the collector. When a collector mesh geometry is used, the airflow can pass through the collector. The resulting airflow can be pointed to a heat sink to increase the heat convection. To evaluate the generated airflow and test the efficiency of ionic winds, a test system was built. The test system is based on the study performed in Knap et al. [101]. For the emitter a tungsten-cerium electrode is used. It was identified as an efficient material in Knap et al. [101]. The electrode has a needle tip with a diameter of 1 mm and a tip radius of 26.5 µm. To enable airflow, the collector consists of a round steal mesh with a diameter

Table 2.7: Measured efficiency of the ionic wind generator

V	$d = 15\,\mathrm{mm}$	$d = 20\,\mathrm{mm}$	$d = 25\,\mathrm{mm}$
4.52 kV	$0.5025\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.2154\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.1452\,\mathrm{m\,W^{-1}\,s^{-1}}$
5.28 kV	$0.5006\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.4114\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.4018\,\mathrm{m\,W^{-1}\,s^{-1}}$
6.03 kV	$0.4802\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.5110\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3837\,\mathrm{m\,W^{-1}\,s^{-1}}$
6.78 kV	$0.4111\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3532\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3285\,\mathrm{m\,W^{-1}\,s^{-1}}$
7.54 kV	$0.4017\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3431\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3159\,\mathrm{m\,W^{-1}\,s^{-1}}$
8.29 kV	$0.3791\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3023\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.2944\,\mathrm{m\,W^{-1}\,s^{-1}}$
9.04 kV	$0.3370\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3008\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.2972\,\mathrm{m\,W^{-1}\,s^{-1}}$
9.79 kV	$0.2996\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.2756\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3150\,\mathrm{m\,W^{-1}\,s^{-1}}$
10.55 kV	$0.2730\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.2736\,\mathrm{m\,W^{-1}\,s^{-1}}$	$0.3042\,\mathrm{m\,W^{-1}\,s^{-1}}$
mean	0.3983	0.3318	0.3096

of 93 mm. Using a needle holder, the distance between emitter and collector can be adapted. The system is supplied by a high voltage generator with an output voltage of 35 kV to 40 kV. The airflow is measured using a hot-wire anemometer (Trotec TA300) which is placed 107 mm apart from the collector mesh. The airflow is measured at different supply voltages in a range from 4.52 kV to 10.55 kV and a distance from emitter to collector of 15 mm, 20 mm and 25 mm. The results of the measurement are shown in Table 2.7. The values are shown in $\mathrm{m\,W^{-1}\,s^{-1}}$ to identify the efficiency. A maximum efficiency of $0.5\,\mathrm{m\,W^{-1}\,s^{-1}}$ is achieved with a supply voltage of 4.52 kV. The use of the area of the airflow calculated by the diameter of the mesh of 93 mm, results in an air volume flow per W of:

$$Q = \frac{\mathrm{d}V}{\mathrm{d}t} = v \cdot A \tag{2.38}$$

$$K = \frac{q}{P} \tag{2.39}$$

$$K = 0.5\,\frac{\mathrm{m}}{\mathrm{W\,s}} \cdot \left(\frac{93}{2}\right)^2 \mathrm{mm} \cdot \pi \tag{2.40}$$

$$K = 0.073\,\frac{\mathrm{m^3}}{\mathrm{W\,s}} \tag{2.41}$$

A standard value of a radian fan noted in the data-sheet [104] is $0.2\,\mathrm{m^3\,W^{-1}\,s^{-1}}$. This leads to the fact that the standard fan is up to three times more efficient. But the speed given in the fan data-sheet is measured directly at the fan output. Conversely, the airflow speed in this experiment was measured 107 mm apart of the ionic wind generation due to safety reasons. After identifying the efficiency of the ionic winds, the cooling effect was

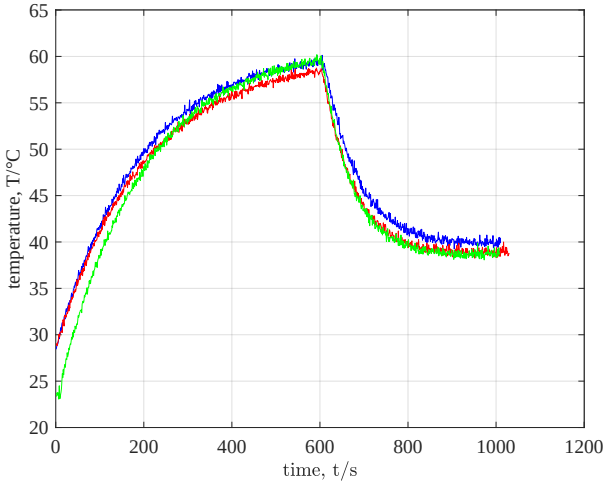


Figure 2.26: Measured temperature of an LED uncooled for 600 s and subsequently cooled by ionic winds with different distances between emitter and collector

tested on an LED by pointing the airflow generated by the ionic wind to an LED with attached heat sink. The hot-wire anemometer was replaced by an LED with attached heat sink. The temperature of the LED was measured using the perilously defined distance between emitter and collector of 15 mm, 20 mm and 25 mm. The LED is supplied by a forward current of 1.5 A resulting in a forward voltage of 4.14 V. Using (2.22) the heat dissipation power for the LED can be calculated as follows:

$$P_t = 0.75 \cdot V_f \cdot I_f \tag{2.42}$$

$$P_t = 0.75 \cdot 4.14\,\mathrm{V} \cdot 1.5\,\mathrm{A} \tag{2.43}$$

$$P_t = 4.67\,\mathrm{W} \tag{2.44}$$

Starting the test, the LED is supplied for 600 s with deactivated cooling. After 600 s the ionic wind is activated. The LED temperature is measured at the surface of the heat sink using a digital thermometer. During the first 600 s, the LED heats up from ambient temperature of ≈23.5 °C to ≈60 °C. The active ionic wind cooling reduces the LED temperature to ≈40 °C. Figure 2.26 shows the temperature of the LED over time for three various distances between emitter and collector. It can be seen, that the distance does not effect the temperature of the cooled LED significantly. Differences around ≈ ± 1 °C resulting in following mean values noted in Table 2.8. The reduction of the thermal resistance of the system can be

Table 2.8: Mean temperatures measured in the ionic wind cooling test

ambient temperature	max temperature	temperature with applied cooling
23.5 °C	60.125 °C	39.91 °C

identified using (2.45).

$$R_{th} = \frac{\Delta T}{\dot{Q}} \tag{2.45}$$

$$R_{th1} = \frac{333.275\,\mathrm{K} - 296.65\,\mathrm{K}}{4.67\,\mathrm{W}} \tag{2.46}$$

$$R_{th1} = 7.84\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.47}$$

$$R_{th1} = \frac{313.06\,\mathrm{K} - 296.65\,\mathrm{K}}{4.67\,\mathrm{W}} \tag{2.48}$$

$$R_{th1} = 3.51\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.49}$$

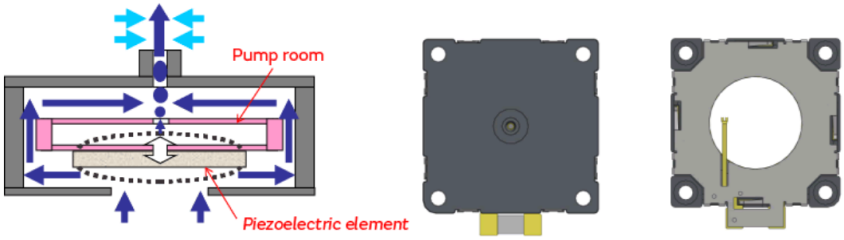
$$R_{thdiff} = R_{th1} - R_{th2} \tag{2.50}$$

$$R_{thdiff} = 4.33\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.51}$$

Result of this test is a reduction of the thermal resistance of ≈55 %. Currently there are a few patents available showing how to use ionic wind to cool LED bulbs. One uses a radial placed ring of ionic wind generators around a heat sink [105], a voltage of 3.5 kV to 4 kV is applied by a distance of 2.52 mm from emitter to collector. Simulations presented in the patent, result in a velocity of 1 m s^{-1} to 3 m s^{-1} and a temperature decrease of an ceramic heat plate from 86 °C to 74 °C. Wei-Min, Jeff WANG, Daniel Jon Schlitz, Ashwini Choudhary, ScottL Gooch [106] introduces an ionic wind fan which can be integrated into the LED bulb. The ionic wind fan can be placed between two heat sinks with small fins in a layer of the LED between heat spreader plate and power supply electronics. Another uses an ionic wind generator inside an LED bulb [106] depicted in Figure 2.30a.

Synthetic jets

Synthetic jets operate based on the fluid-net-mass-flux principle [107]. A jet inhales and exhausts a medium through one or more nozzles. A typical synthetic jet has one nozzle in the centre, the output and an inlet at the opposite side. In general, the airflow is pressed through a narrow nozzle to generate a jet. Luo and Liu [109] shows the basic idea and the geometry to



(a) (b)

Figure 2.27: Schematic of muRata Microblower MZB1001T02 pump (a) and the compound and product picture (b) [108]

create an array of jets. An air pump is used here and the airflow is pressed through a matrix of small nozzles. In contrast to a classic fan providing a constant airflow to move high volumes and to remove heat from a surface, synthetic jets are focused on high speed air streams. They have two advantages compared to a classic fan. The high speed of the air jet removes the thermal border layer on top of the heat sink which increases the cooling and reduces the thermal resistance between heat sink and ambient. Furthermore, they are more efficient because the jet stream can be focused on the heat source and can dissipate the heat directly where it arises. The design of a synthetic jet device by muRata is shown in Figure 2.27. A single jet is generated by creating an ultrasonic vibration of a ceramic fibre which results in an extremely compact, thin and silent device with a high flow rate [108]. Figure 2.27b gives an overview of the project distributed by muRata. The muRata device has to be powered by an AC supply of up to 20 V and a frequency of 26 kHz. muRata offers a driver circuit converting a DC voltage into the required AC voltage. The supply circuit has an internal loss of ≈1 V. The air flow speed ,generated by synthetic jets, is measured with a test system. A hot-wire anemometer is placed next to the output nozzle of the synthetic jet. In Figure 2.28a the resulting air speed in the supply range of the synaesthetic jet is shown. The airflow is generated at a supply voltage of 2 V and a maximum airflow of 21 $\mathrm{m\,s^{-1}}$ can be observed at a supply voltage of 20 V. Figure 2.28b showns the power consumption at the generated airflow. Below 18.7 mW no airflow is created, hence it is the power loss of the driver circuit. Furthermore, a high slope of the airflow can be detected in the range of 58 mW to 196 mW. The efficiency is reduced for higher input power. It can be calculated using the values depicted in Figure 2.28b resulting in a maximum efficiency of ≈27 $\mathrm{m\,W^{-1}\,s^{-1}}$. For the synthetic jets, the efficiency is not measured in $\mathrm{m^3\,W^{-1}\,s^{-1}}$ because the area of air low is small. To compare the synthetic jets with the ionic winds, the synthetic jet was also used to cool an

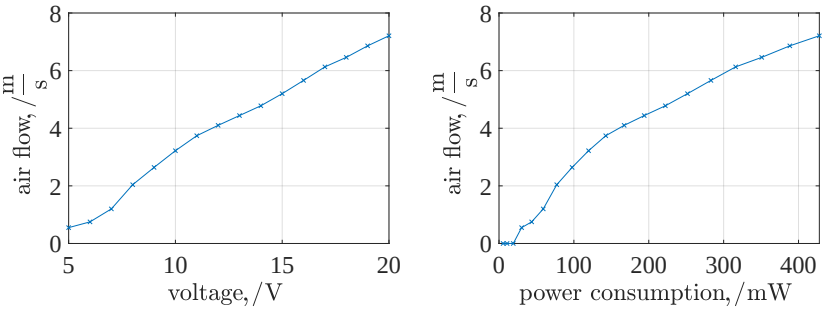


Figure 2.28: Air speed of the synthetic jet in the operation area of 3 V to 20 V (a) and the air speed corresponding to the power consumption (b)

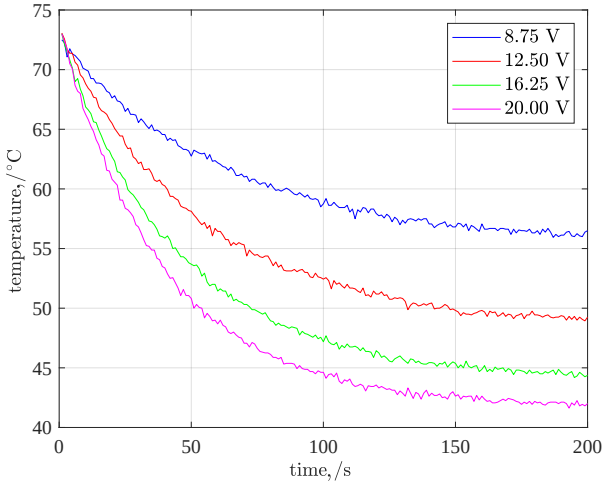


Figure 2.29: Temperature profile using supply voltages of 8.75 V, 12.50 V, 16.25 V and 20.00 V of the synthetic jet with an LED start temperature of 75 °C

LED. As already mentioned, the jet stream created by the synthetic jet has a small diameter. Consequently, the heat sink was detached from the LED and the stream is pointed directly on the LED mounted on a Metal-Core Printed Circuit Boards (MCPCB) to supply and create a slightly bigger surface where the air stream created by the synthetic jet can be aimed at. The cooling test was performed with four different supply voltages of the synthetic jet of 8.75 V, 12.50 V, 16.25 V and 20.00 V. For each test, the LED

was supplied without applying a cooling until it reaches a temperature of 75 °C. Since no heat sink is attached to LED, the supply power was reduced to 2.81 W to avoid overheating. Temperature profile is depicted in Figure 2.29 resulting in a cooled temperature of 55.55 °C, 48.83 °C, 43.83 °C and 41.95 °C for the corresponding supply voltage. The biggest cooling effect occurs at the supply step from 8.75 V to 12.50 V, this supports results from the efficiency test. Linking all results from this test to calculate the thermal resistance of the system using (2.45).

$$R_{th1} = \frac{348.15\,\mathrm{K} - 296.72\,\mathrm{K}}{2.81\,\mathrm{W}} \tag{2.52}$$

$$R_{th1} = 18.33\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.53}$$

$$R_{th1} = \frac{315.1\,\mathrm{K} - 296.27\,\mathrm{K}}{2.81\,\mathrm{W}} \tag{2.54}$$

$$R_{th1} = 6.57\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.55}$$

$$R_{thdiff} = R_{th1} - R_{th2} \tag{2.56}$$

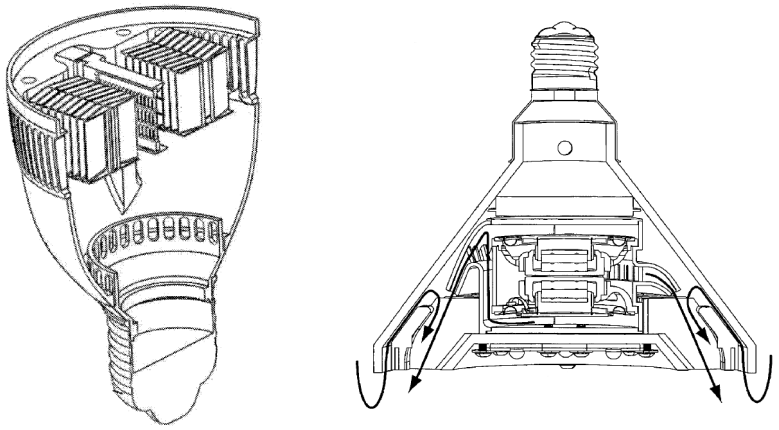
$$R_{thdiff} = 11.76\,\frac{\mathrm{K}}{\mathrm{W}} \tag{2.57}$$

This test results in a reduction of the thermal resistance by ≈65 %. There is also a patent available where synthetic jets are used in an LED bulb as a cooling device [110]. Two ceramics are included into the LED housing as a dual actuator assembly. Ultrasonic vibrations of the ceramic create an air stream pointing to the LED heat sink. The air inlet is placed radial to the LED cover of the housing in a 180° radius. The air outlet is placed on the opposite side of the housing in a 180° radius. The basic geometry is shown in Figure 2.30b.

2.7. Dynamic Thermal Management (DTM)

The thermal management is needed to monitor, adapt or even protect a system against overheating. Current literature describes the attachment of a heat sink to an LED as thermal management [37–42, 75, 111–115]. To develop a DTM for LEDs, thermal management themes of devices with a similar thermal behaviour are analysed to adapt these themes for an usage in LED technology. LEDs are semiconductor devices and microprocessors consisting of materials comparable to LEDs. This is why the thermal management is discussed in this section and is adopted to an LED thermal management.

Current chips and System On Chips (SOCs) on the market have a mechanism to manage supply voltage, clock frequency and cooling based on feedback of an internal temperature sensor. Some commercial chips in-



(a) (b)

Figure 2.30: Solid-state light bulb having ion wind fan and internal HEATSINK (a)[106] and a light fixture with multiple LEDs and synthetic jet thermal management system (b)[110]

clude an additional on-chip thermal management. Early PowerPC processors used a Thermal Assist Unit (TAU) [116], IBM® use an EnergyScale microcontroller for their Power6® and Power7® systems [117], Intel® uses a Thermal Monitor1 (TM1) and TM1 [118] and AMD have developed an on-chip thermal evaluation [119]. These systems are generally called DTM [120]. Basically, the DTM systems adapt the internal power loss to reduce the temperature. For complex processor structures the power loss is defined by the used amount of peripherals, the clock frequency and the supply voltage. The LEDs power loss depends on the forward current. Therefore, the system has to de adopted to change the forward current to reduce the power and therefore reduce the temperature. The implementation of a DTM in chips is mainly driven by a die temperature sensor. For the discussed LED system, the relevance is shifted to the temperature of the active region of an LED. As already shown in Section 2.4.1, the measured temperature is used to adapt thermally relevant parameters. Therefore, the temperature identification is not covered in this section. This section discusses currently used DTMs and how they can be used or adapted in LED technologies.

2.7.1. Early Methods For DTM

Early DTM systems are used in Intel® Pentium™4 and AMD Athlons™family [121, 122]. For example, the first systems used by Intel® are called TM1. They use an internal thermal diode as temperature sensor and implement

an idle time in response to overheat [121]. The internal measured temperature is compared to the maximum temperature ratings (i.e. T_{max},T_{min}) defined in the device data sheet and is subsequently used to calculated the difference between current temperature and maximum rating. Allowed values for the difference are positive values down to 0. If the difference is 0 or close to 0, the thermal management system is triggered. The system has two running modes using this kind of DTM. As long as no temperature threshold is exceeded, the system is running in standard operation mode with maximum clock frequency. If the temperature exceeds the maximum value, a thermal control system is activated. This system stops the clock for a predefined duty cycle until the measured temperature drops below the maximum rating. This system state is held until the device cools down. In the event of a cooling error or other external heating where the thermal management system is not capable to reduce the temperature, the entire system switches to shut-down mode and stops operating if a certain temperature is exceeded, e.g. $T_{max}+20\,°C$. TM1 can either operate autocratically by hardware or can be accessed by software. Early DTM systems used by IBM® in their PowerPC® family are based on an on-chip TAU [123]. This TAU can operate in two states, too. An advantage of this system is that a second step can be included, so the measured temperature can be compared either to one or two thresholds.

2.7.2. Second Generation DTMs

The first DTM methods have evolved over time and have been combined with other power management methods. They have also been adapted and specialised for the upcoming groups of desktop, server and mobile systems. Intel® introduced their second-generation DTM, called Thermal Monitor2 (TM2) in their device family Pentium M for mobile devices [124]. In contrast to the first DTMs which only stop the system clock using a predefined duty cycle scheme, the second generation implements a dynamic voltage and frequency scaling. When the measured temperature exceeds a certain level, the TM2 is activated. The processor speed is adjusted first. The internal Phase Locked Loop (PLL) is locked to a lower frequency. When the frequency is stable, the voltage is reduced in steps of approximately $1\,mV\,\mu s^{-1}$ to fit the new frequency. A possible implementation is based on a list of reduced frequencies and the corresponding voltages. While the Thermal Monitor (TM) is active, the temperature is measured and reported to the TM. The TM constantly checks whether the temperature is reduced below the threshold or if it is still rising. If the temperature is reduced below the threshold, the TM stops and the processor starts to operate in the normal operation mode. However, if the temperature still rises, the TM steps into a lower frequency voltage configuration. Similar to TM1, the system switches to ”power off” if the temperature still rises in the lowest frequency voltage configuration. IBM® introduced the En-

ergyScale technology for its dual-core Power6® processors [125]. They used a special microcontroller to take over the thermal management which is called Thermal and Power Management Device (TPMD). The TPMD is responsible for the on-chip thermal management as a pure software solution enabling rapid run time response to thermal events. Two so called capping schemes are implemented. The first is a thread-level pipeline throttling and the second is frequency and voltage scaling, they can be used separately or simultaneously. If the TPMD recognises a temperature increase, the core dispatch rate is reduced until the temperature falls again. The second method available to reduce the chip temperature is reducing the core clock frequency and the supply voltage respectively.

2.7.3. Latest Generation DTMs

Current versions of DTMs do not only reduce the system parameter to prevent the internal overheating, they also have utilised a boost mode. This boost mode allows the processor to increase its frequency to increase the system speed if sufficient thermal reserve is available. An example for this technology are the IBM® Power8® and Power9™thermal management and the AMD Hybrid (HY) boost and Configuration Thermal Design Point (TDP). IBM® developed its EnergyScale technology to be used in newer processors. They named it EnergyScale microcontroller used for power and thermal management. A total of 44 Digital Temperature Sensors (DTSs) have been integrated into the 8-core processor, 5 per core and 4 for the peripheral. One novelty of the new EnergyScale system is the ability to scale the clock frequency for an individual core. Every core has an own fractional digital PLL, which can be controlled by the EnergyScale microcontroller. The IBM® processor Power8®, built on the 22 nm technology, uses an on-chip controller for power and thermal services [126]. A new member of the IBM® family is the IBM® z14®, produced in the 14 nm technology containing 10 cores [127]. Similar to EnergyScale, International Business Machines Corporation (IBM) has implemented a throttling to limit the temperature of the processor. Throttling is activated by a DTS and by a Critical Path Monitor (CPM). An extensive characterisation is needed to set the throttle threshold as well as the throttle magnitude. To avoid errors, the duration results have to be considered in the thermal control loop [127]. Intel® uses a hight thermal design power in its Xeon® processors which is accompanied by a lot of challenges for current cooling technologies [128]. In their new architecture called Syklake they introduced a wider and deeper power-efficiency enhancing the performance of lower-thermal-power [129]. Their new thermal management is based on the previously developed TM1 and TM2 [130]. One modification is that the temperature limit for throttling has been elevated compared to previous systems [120]. This helps to reduce the variability in the absolute throttling trigger level across different processors. As soon as a spe-

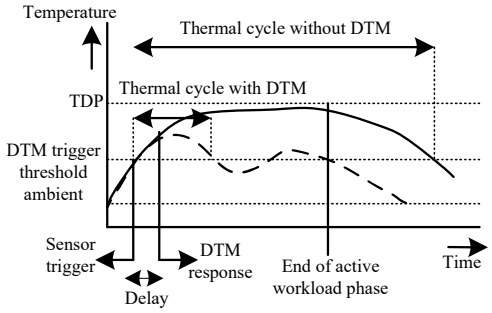


Figure 2.31: The impact of DTMs response delay on the thermal state of a system [120]

cific thermal management scheme is activated, the temperature sensors are interfaced with an on-chip embedded thermal management circuitry which is referred to as the DTS circuitry. This autonomous hardware unit can execute TM1 or TM2 previously introduced in the older Pentium 4 and Pentium M families, respectively. TM1 and TM2 can both be enabled and disabled by the Basic Input Output System (BIOS). For system-level management, the Platform Environment Control Interface (PECI), an Intel® proprietary interface is used to communicate the thermal state of the chip.

2.7.4. Control Systems For DTM

DTM with on-chip temperature sensors and a feedback loop detect the hottest on-chip temperature which represents the overall thermal state of a chip. The response mechanisms, i.e. performance throttling, dynamic voltage and frequency scaling are core-wide or chip-wide. Over the last two decades, DTM evolved into an active research field to scale system parameters by still meeting calculation deadlines [131]. Figure 2.31 shows how a basic DTM affects the processors state and active time. These DTMs are based on different control systems. A thermal control system consists of the temperature sensor at a critical chip position and a feedback system with an included control unit. The control unit can consist of a closed loop feedback controller and a Model Predictive Control (MPC). A closed loop controller uses the feedback of the critical system state to control the system. In the case of an LED, it is the junction temperature. The control system reacts on a rise in temperature and adjusts system parameters to reduce the temperature. System parameters are forward current for an LED or supply voltage and clock frequency for a microprocessor. The major parts of an closed loop controller are an reference input R, the error evaluation and response generation as part of the controller, the device

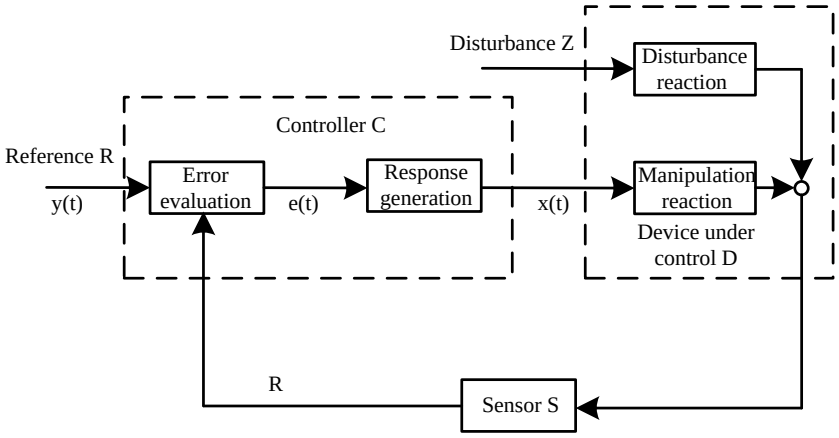


Figure 2.32: Typical feedback control loop with controller and device under control (plant) [132]

under control D with an external disturbance input and a sensor as shown in Figure 2.32. For an microprocessor, the reference input could be the threshold temperature for throttling. For an LED it could be the maximum operation temperature. The error evaluation e calculates the difference between the currents sensor value and the reference value. The resulting difference is transmitted to the controller which controls the device under control in such a way that the error is reduced.

Proportional Integral Derivative (PID) Controller

The most common controller design is a Proportional Integral Derivative (PID) controller. The transfer function of the controller describes the response to the calculated error e. A (P) controller is the simplest controller type where the output of the controller is proportional to e. This can be enhanced by including the integral of the error e. This gives a better conversion at low errors e. The resulting function of the controller can be written as following:

$$u(t) = K_P \cdot e(t) + K_I \int e(t)\, dt \tag{2.58}$$

$$e(t) = y(t) - R \tag{2.59}$$

The resulting controller is called (PI) controller, its Laplace transformation of the system is given in (2.60).

$$U(s) = K_P + \frac{K_I}{s} \tag{2.60}$$

The controller can be extended by adding the derivative of the error e which will smooth the response. The derivative will react to changes to reduce overshoot or undershoot of the controller. The resulting transfer function is given as:

$$u(t) = K_P \cdot e(t) + K_I \int e(t)\,dt + K_D \frac{de(t)}{dt} \tag{2.61}$$

$$U(s) = K_P + \frac{K_I}{s} + K_D s \tag{2.62}$$

Skadron et al. [133] implemented the so-called (PID) controller to manage the temperature of an microprocessor changing the system clock frequency, while Donald and Martonosi [134] and Kadin et al. [135] cancelled the derivative component and used the (PI) controller. Donald and Martonosi [134] observed that the derivative part is insignificant for thermal management in Integrated Circuits (ICs) and Kadin et al. [135] determined that the derivative part results in noisy output of the controller.

Linear Quadratic Regulator (LQR) Algorithm Controller

Another method to control the temperature of an IC is the usage of an Linear Quadratic Regulator (LQR) algorithm. It is based on the state-space representation of the system and can be expressed with (2.63) and (2.64) [120].

$$x[n+1] = Ax[n] + Bu[n] + N\phi[n] \tag{2.63}$$

$$y[n] = Cx[n] + Du[n] + \sigma[n] \tag{2.64}$$

Where $x[n]$ represents the state of the device under control (i.e. temperature), $u[n]$ represents the input of the system, i.e. voltage and frequency and $y[n]$represents the output of the system. In (2.63), $\phi[n]$ represents the inaccuracy of the modelled system and in (2.64) $\sigma[n]$ represents noise in the feedback path of the controller. A DTM implemented using a LQR is shown by [136]. The designed system is used to control the operation frequency of an processor to its optimal performance-power in consideration of the thermal state of the processor. They defined a cost function for the LQR defined as (2.65).

$$J(u) = \sum_{k=1}^{\infty} [x(k)^T Q x(k) + u(k)^T R u(k)] \tag{2.65}$$

In (2.65) Q is related to the thermal consequence of the controller output while R represents the power consumption of the device. Both terms can be weighted using the weights to adapt the importance. The result of the study is an increased performance of 32.84 % compared to other per-

formance studies. Furthermore, temperature changes are limited to 2 °C for 66 % of the runtime which is eight times more than the best thermal balancing technique [136].

2

Stochastic Control

The uncertainty of the temperature measurement device for ICs and the noise overlaid by the conversion circus and the communication interface lead to a stochastic description of the controller input [120]. Therefore, DTM problems have been solved applying stochastic control. Stochastic control describes the observed state of the system as arbitrary. The objective of the controller is to minimise the difference between the observed chip temperature and the temperature limit. One possible implementation of stochastic control is the Makovian process. It describes the control system as a number of finite states. Each state has a defined number of transition conditions to a number of other states. The Makovian process includes two components, the action and the cost of the transition between two states. The Transition Probability (TP) is subsequently determined by a global distribution, a specific action and an associated reward. It describes the probability of a transition from a current state into another. The controller's task is, to find the next state with lowest cost. One possible solution is to check the costs of each possible change and check which one has the lowest costs. In the application of DTM, each state represents a thermal condition of the system. Unfortunately, these thermal conditions are infinite and cannot be represented in a finite number of states. Therefore, the desired operation temperature is divided into sub ranges [137]. An example is shown in Figure 2.33 where the overall operation rage is defined as 50 °C to 90 °C. The range is divided into three sub ranges, 50 °C to 65 °C, 65 °C to 75 °C and 75 °C to 90 °C. The thermal manager can choose from a finite set of actions, for this example the supply voltage and the clock of the processor can be manipulated to prevent overheating. Jung and Pedram [137] complemented the system with a state observer to identify upcoming states resulting in a POSMDP. The observer determines a probability of the system to change its state when an action is performed.

2.7.5. DTM For LEDs

After identifying promising DTM methods and its controller types, a thermal management for LED systems must be deducted. For a complex system consisting of more than one LED the complex DTMs can be used, where each LED can be used as a single temperature source. Nevertheless, the LED has only one system parameter which can be changed to reduce the internal generated heat, the forward current. But an LED array containing more than 10 LEDs is comparable to the complex structure of a microprocessors. For example a PID or even an adopted LQR Algorithm Controller

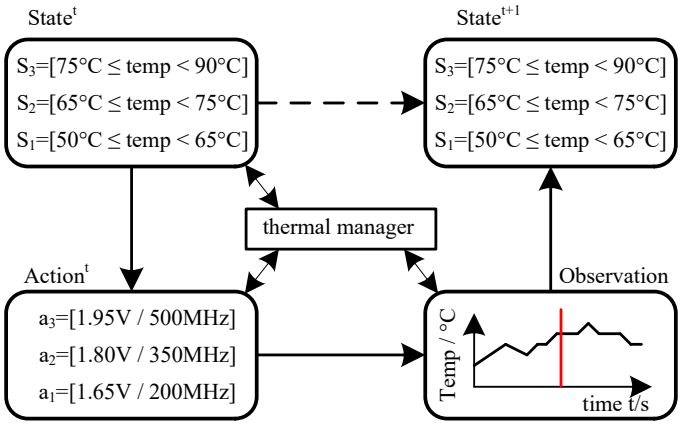


Figure 2.33: Partially Observable Semi-Markov Decision Process (POSMDP) framework for the dynamic thermal management [137]

can be used to control temperature hotspots as well as the colour and light quality of an LED array.

A single LED, which is used in this work has a straightforward structure and an approximately homogeneous temperature distribution, compared to a multi-core microprocessor. The most promising thermal management of a simple system consistent of one LED and its supply is a Semi-Markov Decision Process (SMDP). The LED can operate in three major ranges, standard operation range from room temperature to its standard operation junction temperature e.g 20 °C to 85 °C (S_1), in high operation temperatures from standard operation temperature to the defined maximum junction temperature, e.g. 85 °C to 150 °C (S_2) and in the overheating state for temperature >150 °C (S_3) [88]. If the LED state is S_1, the LED can be supplied up to its maximum forward current, if the LED changes its state to S_3, the supply has to be stopped to prevent critical temperatures and resulting damage of the LED, the so called thermal shutdown. The state S_2 ranges form a standard operation temperature up to maximum temperature and can be divided into sub states.

A similar thermal control function for LEDs was proposed by [138] where stage S_2 is designed as a linear function. Texas Instruments Inc. also uses such a three stage design for the LED driver LM3464. Here, stage S_1 is the standard operation, when the threshold temperature is exceeded, the forward current of the LED is reduced linearly up to 0.5 % of the standard current[139]. If light output has to be guaranteed, the supply can be changed to ≈10 % of the desired forward current. Another problem occurs if the LED is turned off completely: no temperature measurement is possible using the forward voltage method with a current low through the

LED. This means that the driver cannot change back from S_3 by itself and needs an external reset signal. Four possible methods have been identified which can be implemented to avoid or overcome this fact. The first is to drive the LED with the minimum current needed to determine the temperature of the LED using the forward voltage method. The second uses the modified PJTM where in difference to the standard PJTM operation, a short current pulse is provided to detect the temperature and the LED is turned off in between. As a third method, the LED driver gets a periodical external reset: if the temperature is still in the range of S_3, the LED will switch back into S_3, otherwise it will operate in the current state related to its current temperature. According to the last possible methods, the driver will stay in the thermal shutdown mode S_3 until it gets an external reset to change back into another mode defined by the current detected temperature.

For example the reset will change the mode into a S_2 or S_1 depending on how fast the temperature moved from S_1 to S_3. It has to be mentioned that the LED will not reach S_3 mode by self heating if it is supplied with a working DTM. An active DTM will reduce the forward current in such a way that the LED will be held under its maximum operation temperature. The S_3 mode can only be reached when the LED is heated by an external source.

2.8. Summary

In this chapter, the important characteristics of white light LEDs are presented. The basic light emitting physics are introduced as well as the possibilities to create white light using LEDs. The most commonly used technology to create white light is a blue LED combined with a colour conversion layer, i.e. phosphor. The phosphor shifts a part of the blue light into yellow resulting in an addition of blue and yellow light which has a white light appearance in the human eye. Possible LED phosphor combinations are listed and advantages and disadvantages are shown. Afterwards, the structure of LEDs is described. A MQW structure which can increase the Internal Quantum Efficiency (IQE) is shown followed by a list of possible LED dome structures. The LED structure section is concluded by a description of up to date packages for LEDs.

Followed by the structural distribution of LEDs, the thermal behaviour of LEDs is shown. Starting with the efficiency and internal created heat, possible temperature determination methods are analysed. The forward voltage method was identified as the most suitable method to identify the junction temperature of an LED without using external measurements. Three variations of the method are described in detail: the linear, quadratic and pulsed method. The quadratic approach determines the junction temperature best, but uses the most complex calculation and will therefore use most resources. The pulsed and linear were determined as best

fit for an ASIC development, because of relatively simple algorithms. For the pulsed forward voltage method a more complex calibration has to be performed and the timing has to be maintained regarding [76] what makes the LED drive more complex. Furthermore, pulsed currents on the LED can result in bead string artefacts or flickering [140] which reduces the light quality. To calibrate the forward voltage method with an LED in a experiment, a current pulse source was developed. This calibration setup creates a short current pulse with a length of 5 µs and an adjustable current of 0.1 A to 1 A. In the CIE225:2017 [76] it was identified that no self heating of the LED occurs when it is supplied for such a short duration. Furthermore, the TTE is considered for the calibration.

After identifying a method for the junction temperature determination, multyphysic simulations of LEDs are performed to simulate the thermal distribution in the LED. The simulations using the COMSOL simulation tool start with a simple junction model of an LED. The models become more complex up to the simulation of an up-to-date LED from CREE®, the CREE® XLamp® XP-L High Intensity LED. The geometrical structure of the LED was determined by an electron microscope image. The simulation results are compared to experimental results using the InfraTec ImageIR 8380S IRCamera. Hence, the simulation results and the experimental results fit well, the internal temperature especially the temperature of the phosphor was extracted from the simulations. It was considered if the forward voltage method can also be used to determine other temperatures inside the LED except the junction temperature. Since temperature differences near to the junction of the LED are low, the forward voltage method can also be used to identify temperatures near the junction, e.g. the phosphor temperature or the temperature of the transition from phosphor to the dome.

After analysing the internal temperature of LEDs using multiplicity simulations, cooling mechanisms are investigated. Starting with standard cooling systems using a heat sink combined with a fan, new low noise approaches such as synthesis jets and ionic winds are analysed in terms of efficiency and applicability. As a result, current patents of the two systems related to LEDs are introduced.

To combine the LED with a temperature determination and a cooling system, DTMs are discussed. Currently used thermal management systems for microprocessors are investigated to developed a management system for LEDs. First versions of DTMs are introduced followed by the description of latest generation of DTMs including control systems. The DTM section is concluded by adopting a suitable DTM for an LED system. For a single LED the approach is applicable which reduces the supply current successively if the temperature is rising above a predefine threshold. When the junction temperature exceeds a maximum temperature rating, the LED is turned into a thermal shutdown mode (S_3). Furthermore, it was identified that an LED

cannot reach the thermal state $S_3$by selfheating with a working DTM. In the thermal shutdown mode (S_3) no temperature measurement is possible, therefore four different possible methods were identified to allow the DTM activating the LED again.

3

LED Driver

If you really want to understand something,
the best way is to try and explain it to someone else.

Douglas Adams

This chapter describes LED driver topologies. Currently a lot of LED drivers are available on the market. They can be grouped into four major application fields: lighting applications, status indication of electric systems, automotive and mobile devices. Lighting applications comprise private house lighting, public building lighting and industrial lighting. In most cases the LED drivers for lighting applications are supplied by the electric supply grid, e.g. 230 V AC, 50 Hz to 60 Hz. In contrast, electric systems with a status indication have an integrated voltage regulator. The indication LED driver is supplied by ≤24 V DC. In the automotive industry the supply voltage is 12 V or 24 V. Mobile devices with a small battery, e.g. mobile phones or camera are supplied by 2 V to 5 V. To cover this large range of application, many different types of LED drivers are available. The none linear relation of forward voltage and current is described as the characteristic curve (Figure 2.10). An LED has to be supplied with constant or controller DC current to be operated in a stable condition. Therefore, an AC-DC converter is needed to supply the LED from the power line. This chapter starts by introducing LED driver topologies for AC and DC supplies and will subsequently give a detailed description of linear drivers followed by step converters and new approaches. This chapter will also show the used LED driver topology in this study and its design. To supply the LED with a constant current, the LED current has to be controlled by a current controller. The controller design is performed by identifying the system of the used typology including the LED load.

3.1. Driver Topologies

Supply topologies for a DC system can be grouped in AC/DC and DC/DC converters. In most cases AC/DC converters consist of a rectifier with a DC/DC converter in series. DC/DC converters can be divided into two groups, linear supplies and switching supplies. Depending on the supply voltage and on the operation area of the LED the best fit LED driver has to be chosen. Important data of voltage regulators are:

- Output voltage value and its tolerance
- Maximum output current and the short-current
- Minimum voltage drop across the controller ”Dropout-Voltage”
- Power loss and efficiency
- Control speed
- Size of PCB and amount of external components
- Line rejection
- Load rejection

3.1.1. Linear Driver

Linear drivers use a controllable resistor in series for an almost constant voltage. The resistor is controlled in such a way that the output voltage stays constant for varying loads. The simplest linear driver is an emitter follower where the base of the transistor is connected to a reference voltage source. The output voltage can be described as (3.1) [141].

$$U_a = U_{ref} - U_{BE} \tag{3.1}$$

By adjusting the feedback from a voltage reference to a current, the linear voltage regulator can be used to provide a constant current. The reference voltage input is connected to an LED current shunt. The voltage drop through this shunt represents the current flow through the LED and subsequently the regulator will therefore control the LED current. Linear drivers are easy to developed and consist of a few parts only. A disadvantage is the low energy efficiency which varies between 25 % and 50 % in most cases. The load current flows through the linear driver and creates ohmic losses which are proportional to the square of the current. This leads to a high power loss (3.2) and to a cooling problem respectively. To reduce the losses and ensure a higher efficiency clocked converters are introduced below [141].

$$P_{loss} = P_{in} - P_{out} = \left(\frac{1}{\eta} - 1\right) \cdot P_{out} \tag{3.2}$$

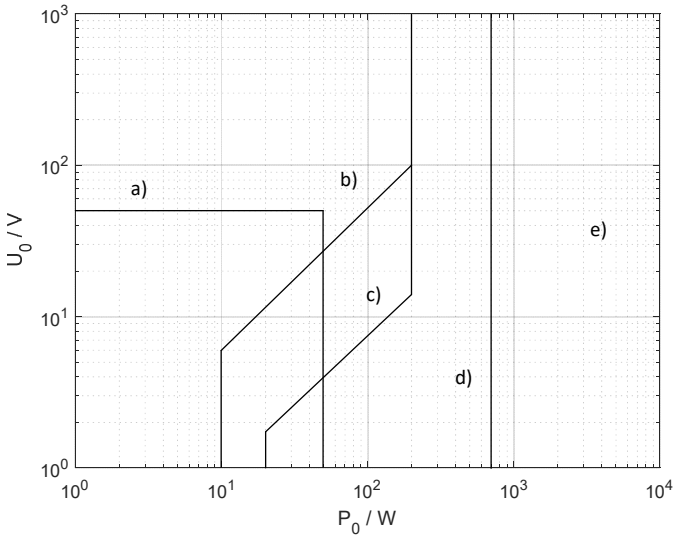
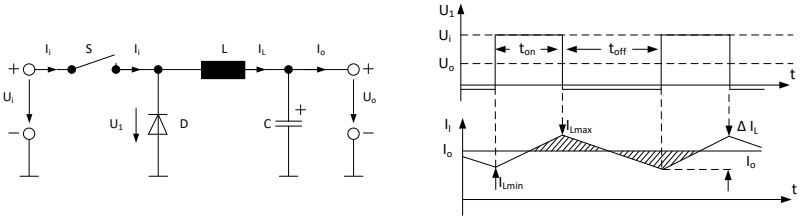


Figure 3.1: Schematic correlation of different step converter with approximate limitations [142]

3.1.2. Step Converter

The losses of the linear drivers can be reduced by replacing the linear controlled transistor by a switch. Before designing a step converter, the needed type has to be identified. Figure 3.1 gives an overview of converters used in different power and voltage regions. Region a) 50 V and 50 W, with relatively low power, thus step-down converters are used. Flyback converters are used in region b) 1000 V and 10 W to 100 W. Region c) 1000 V and 20 W to 100 W is the transition from flyback converters to single transistor forward converters which are used in region d) 1000 V and 200 W to 300 W only. To achieve higher output powers above 300 W in region e) it is reasonable to use a number of single transistor forward converters in parallel.

The basic design of a step-down converter is shown in Figure 3.2a. The switch connects and disconnects the supply from the load periodically and is typically controlled by a pulse-modulated clock signal. A low-pass filter which gives temporal average connected in series provides the desired output voltage. The filter consists of an energy storage element, i.e. an inductor, where the electrical energy is converted in magnetic energy and stored during the switch-on stage of the switch. When the switch is turned off, the magnetic energy of the inductor is transformed back into electrical energy and transferred to the output capacitor. By adjusting the duty cycle of the switch, the output voltage can be changed. Using an LC-



(a) (b)

Figure 3.2: Step-down converter with simple switch and diode [141] (a) and Voltage and current curve of the step-down converter [141] (b)

lowpass, no systematic source of losses is included in the system [141]. The schematic voltage and current curve can be seen in Figure 3.2b. As long as the switch is closed, the voltage U_1 is equal U_i. As soon as the switch opens, the voltage across the inductor U_L is reduced until the diode starts to conduct. The inductor current maintains its direction and thus its time dependence is given by law of induction:

$$U_L = L \cdot \frac{\mathrm{d}I_L}{\mathrm{d}t} \tag{3.3}$$

While the switch is closed ton, the voltage across the inductor is $U_L = u_i - U_o$, while the switch when turned off the voltage across the inductor is $U_L = -U_o$. This results in a current variation of:

$$\Delta I_L = \frac{1}{L} \cdot (U_i - U_o) \cdot t_{on} = \frac{1}{L} \cdot U_o \cdot t_{off} \tag{3.4}$$

The inductance is determined in such a way that the output current does not fall below the minimum required output current $I_{o,min}$:

$$L = T\left(1 - \frac{U_o}{U_e}\right)\frac{U_o}{2I_{o,min}} \tag{3.5}$$

The maximum inductance current as well as switch and diode current is defined as $IL, max = I_o + I_{o,max}$. The period of the switching signal is the only free parameter left. A high frequency f will allow to use a small inductance, higher frequencies, however, will increase the schematic drive effort and will lead to higher switching losses. Due to this, a switching frequency of 20 kHz to 200 kHz is preferred. The smoothing capacitor reduces the output ripple. The charging current is $I_c = I_L - I_o$ which is

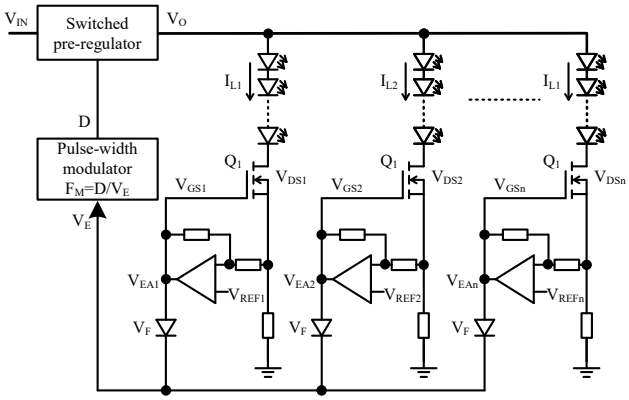


Figure 3.3: LED driver with a switching voltage pre-regulator and detection circuit for minimum voltage drop of linear regulators [143]

equal to the shaded area shown in Figure 3.2b.

$$C = \left(1 - \frac{U_o}{U_e}\right) \frac{T^2 U_o}{8 L \Delta U_o} = \frac{T I_{o,min}}{4 \Delta U_o} \tag{3.6}$$

3.1.3. New Driver Approaches

Current LED drivers for LED arrays combine a stepped converter with a linear converter. An LED array consists of multiple LED strings connected in parallel. The step converter provides sufficient forward voltage for the LED string with the highest resistance. Each LED string has a linear converter in series which controls the forward current of the LED string [143]. The schematic structure of such a system is shown in Figure 3.3. It consists of a pre-regulator and a linear current controller in each LED string. The current ($i = 1, 2, ..., n$) by which each string is controlled is measured with a shunt resistor and comparing it to a reference voltage using an error amplifier. The error amplifier output voltage is the V_{gsi} for the corresponding string and controls the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) which manipulates the desired string current I_{Ln}. All error amplifier outputs are ORed via diodes to identify the highest voltage drop. This voltage drop is used to adjust the switch pre-regulators output voltage to an optimal value. Figure 3.3 shows a pulse width modulator changing its duty cycle D corresponding to the desired output voltage. Alonso et al. [144] describe an IDBB converter for LED supply which can be connected to the 230 V line directly. Figure 3.4a shows the schematic

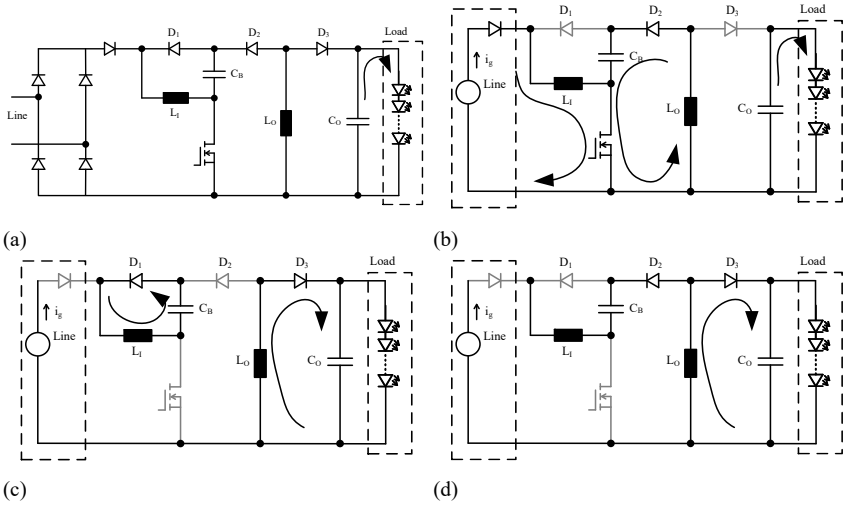


Figure 3.4: Schematic of an IDBB converter (a) and its equivalent circuits for the operations. (a) Interval I: $0 < t < DT_S$. (b) Interval II: $DT_s < t < DT_S + t1$. (c) Interval III: $DT_S + t1 < t < T_S$ [144]

of an IDBB circuit. The IDBB circuit behaves like two cascaded buck-boot converters with L_i, D_1, C_B and M_1 as input buck-boost and L_o, D_2, D_3, C_o and M_1 as output buck-boost. Resulting in a negative voltage in the capacitance C_B corrected to a positive voltage in the capacitance C_o. When operating L_i in Discontinuous Current Mode (DCM), the average current through the line will be proportional to the line voltage resulting in a near unity Power Factor (PF). L_o can operate either in DCM or in Continuous Current Mode (CCM). For a duty cycle lower than 0.5, the system operates in buck mode, for a duty cycle higher than 0.5 it operates in boost mode. Figure 3.4 explains IDBB converter currents and voltages in the switching interval. Figure 3.4b I: $0 < t < DT_S$, Figure 3.4cinterval II: $DT_s < t < DT_S + t1$, Figure 3.4d interval III: $DT_S + t1 < t < T_S$. A novel LED driver with a minimum of active parts is described by Lee et al. [145]. They included a passive LED driver, an LC^3. According to [146] switching LED drivers which use a controller for the PWM and a switch typically have large power loss and a low lifetime compared to the LED. Their objective is to reduce the active parts of an LED driver such as microcontroller and switched controllers. With the introduced LC^3, shown in Figure 3.5, an efficiency of up to 96.7 % is achieved when 90 LEDs are connected to the output. Furthermore, by using an LC^3 filter, they achieve a power factor of 0.95. A problem of the system is that a variation of the input, i.e. line voltage and frequency changes the current through the LED because no controller is included. An improvement of this system was

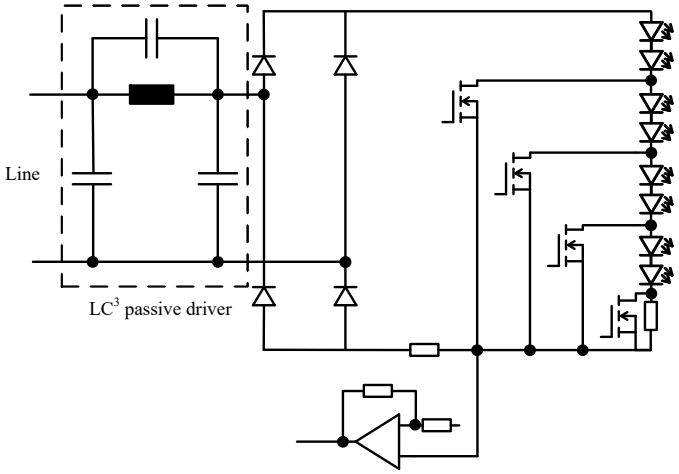


Figure 3.5: Overall circuit configuration of the proposed LED driver for five stage switching circuits [145]

later introduced by Lee et al. [145] where an LED string array is connected to the output of the LC^3 filter, also shown in Figure 3.5. Each string can be shorted by a MOSFET to reduce the load. The basic idea is the dynamic control of the load when the supply is activated. Initially only one string is connected as load and the other strings are shorted. If the supply voltage exceeds a predefined threshold, the other strings are connected step-by-step. This procedure can also be used if the supply voltage changes over time. If it falls below the predefined threshold again, a string can be deactivated. Even if the LC^3 filter does not provide a continuous voltage because of supply variations, strings can be activated or deactivated periodically.

3.1.4. Inductor Less Approaches

All previously discussed LED drivers, except the linear drivers, have an inductor included into their schematic. The inductor cannot be integrated into the driver chip and is the biggest external device needed for the LED driver. To create a full integrable LED driver with minimised external devices, the inductor has to be replaced. In current literature two main concepts are discussed. The first concept uses only capacitors to store the energy, these converters are called charge pump converters. Abraham et al. [147] introduced a novel multiple gain inductor less buck-boost DC-DC converter using only capacitors and switches. They developed a circuit of two capacitors which can be connected in all possible variations using

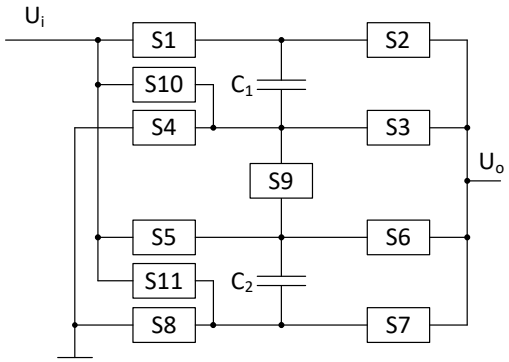
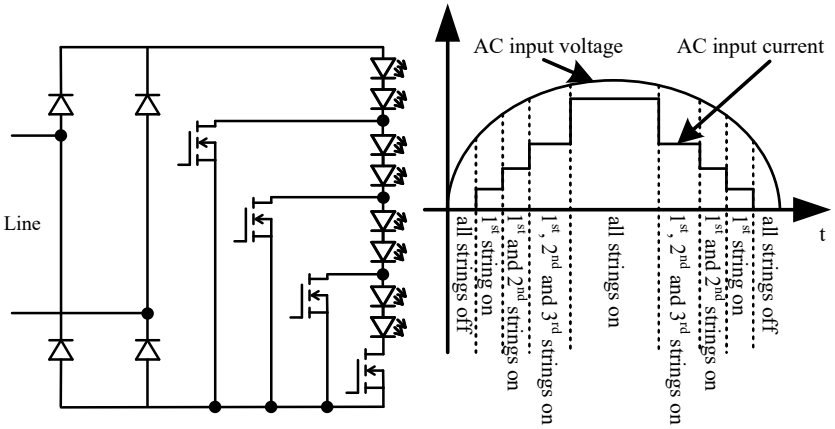


Figure 3.6: Schematic design of the multiple gain topology including 11 switches and two capacitances [147]

Table 3.1: Output parameter of the multiple gain inductor less buck-boost DC-DC converter [147]

VCR (gain)	Output voltage V/mV	Output current I/mA	Output power P/mW
3:1	4	14.8	59.25
2:1	6	22.2	132
3:2	8	29.6	232
1:1	12	44.4	532.8
2:3	18	66.7	1200.8

10 switches. Possible gain configurations are 3:1, 2:1, 3:2, 1:1 and 2:3, the schematic design is shown in Figure 3.6. For a desired input voltage of 12 V, the circuit output voltage can be 4 V, 6 V, 8 V, 12 V and 18 V. Abraham et al. [147] also performed tests to identify the output parameter of the system. Table 3.1 indicates the results of this test. They used capacitors with a capacitance of 2.2 µF, a switching frequency of 2 kHz and a load of 270 Ω. It can be recognised that the maximum output power of 1.2 W is not sufficient for the LED used in this work. The output power can be increased by increasing the switching capacitance and the switching frequency. Examples of LED drivers based on charge pumps are produced by Linear Technology®. The LTC3216 also uses two capacitances of 2.2 µF to boost the supply voltage up to the power of two. It delivers a maximum output current of 1 A by a maximum output voltage of 5.1 V. With these values it can supply a single LED using a switching frequency of 850 kHz to 920 kHz. The efficiency of the driver depends on the input-output voltage



(a) (b)

Figure 3.7: The circuit diagram of a four-step linear driver (a) and AC input voltage - AC input current waveform and the operation of each LED string (b) [148]

relation and can range from 50 % to 95 %. For a LED supplied by the line, Guoxi Sun et al. [148] introduced a novel LED light engine with no inductor or capacitor distributed by Disclight™. The driver consists of a full-wave rectifier without smoothing capacitor which results in a sin output voltage with a ripple double the input frequency. The output voltage is connected to a multi-stage switching circuit. In the example of Guoxi Sun et al. [148], the multi-stage switching circuit includes four LED strings in series. Each string can be short-circuit by switches, Figure 3.7a shows the principle circuit. Depending on the value of the supply voltage, different numbers of strings are connected to the supply voltage. In this example, the system consists of four strings. If the supply voltage is too low to supply one string, all strings are disabled. When the supply voltage reaches a value high enough to supply one string, one string is connected and so on. In the peak of the rippled supply voltage, all strings are connected in series to the line. For the falling supply voltage, the process is repeated backwards. The supply voltage vs supply current diagram is shown in Figure 3.7b. The amount of connected strings is also shown in Figure 3.7b, the steps can be identified clearly. The process shown in Figure 3.7b is performed 100 times per second. The change in luminance will not be reconsigned because of the human eye persistence of vision. A further advantage of this driver is that current and voltage are in phase and therefore the power factor is close to 1. A Problem arising in this topology is that the 1st string is nearly always active and the 3rd string is only active for 30 % of the time. The system has to be changed in such a way that

the arrangement of the strings can be changed to ensure a balanced active time for all LEDs.

3.2. Used Driver Topology

In this project only a single LED with a power of up to 12 W will be supplied and controlled. Figure 3.1 shows the schematic correlation of different step controller types with their corresponding limitations. The step-down converter does fit best for the power of 12 W. The constant current and its maximum variation needed by the LED determine the size of the inductor as shown in (3.5). The supply voltage is given as $U_i = 5V$ and the approximate output voltage is given from the data sheet of the CREE® XLamp® as 2.95 V to 3.25 V [88]. The step-down converter is designed using the equation from [142]. The inductance can be determined using:

$$\Delta I_L \cdot L = (U_i - U_o) * t_1 \qquad \vartheta_T = \frac{t_1}{T} \tag{3.7}$$

$$= \frac{(U_i - U_o) \cdot \vartheta_T}{f} \tag{3.8}$$

$$= \frac{(U_i - U_o) \cdot U_o}{U_i \cdot f} \tag{3.9}$$

Where ΔI_L is the current ripple, L is the inductance, U_i is the input voltage, U_o is the output voltage and t_1 is the duty cycle of the switching transistor. (3.9) results in a lower limit of the inductance of:

$$L \geq \frac{(U_i - U_o) \cdot U_o}{\Delta I_L \cdot U_i \cdot f} \tag{3.10}$$

The inductance should not be too big to reduce the settling time T_e for a load step. T_e can be approximated using:

$$T_e \approx (5 \ldots 20) \cdot T \tag{3.11}$$

An upper limit of the inductance can be calculated using:

$$L \leq \frac{U_o}{\Delta I_{0max}} \cdot t_e \cdot \left(\frac{\vartheta_{Tmax}}{\vartheta_{T1}} - 1 \right) \tag{3.12}$$

The forward voltage of the used Schottky-Diode 0.5 V and the voltage across the MOSFET 0.2 V must be added to the voltage of the LED of 2.95 V to 3.25 V which results in a diode voltage of 3.65 V to 3.95 V. The given parameter result in the following values:

$$\vartheta_{Tmax} = \frac{3.95\,\text{V}}{5\,\text{V}} = 0.79 \tag{3.13}$$

$$\vartheta_{Tmin} = \frac{3.65\,\text{V}}{5\,\text{V}} = 0.73 \tag{3.14}$$

$$T = \frac{1}{f} = \frac{255}{200\,\text{MHz}} = 1.275\,\mu\text{s} \tag{3.15}$$

$$t_{1min} = \vartheta_{Tmin} \cdot T = 0.73 \cdot 1.275\,\mu\text{s} = 0.93\,\mu\text{s} \tag{3.16}$$

$$t_{1max} = \vartheta_{Tmax} \cdot T = 0.79 \cdot 1.275\,\mu\text{s} = 1\,\mu\text{s} \tag{3.17}$$

Using (3.10):

$$L \geq \frac{(5\,\text{V} - 3.65\,\text{V}) \cdot 3.65\,\text{V} \cdot 255}{300\,\text{mA} \cdot 5\,\text{V} \cdot 200\,\text{MHz}} = 4.2\,\mu\text{H} \tag{3.18}$$

Using (3.12) respectively with estimated $\vartheta_{T1} = 0.74$:

$$L \leq \frac{3.95\,\text{V}}{500\,\text{mA}} \cdot 121.275\,\mu\text{s} \cdot \left(\frac{0.79}{0.74} - 1\right) = 8.17\,\mu\text{H} \tag{3.19}$$

Therefore, the inductance has to be chosen between 4.2 H to 8.17 H. A shielded inductance with a high level of availability is the 6.8 µF inductance. The output capacitance of the step-down converter can be calculated using:

$$C_o \geq \frac{\Delta Q}{\Delta U_o} = \frac{\Delta I_L}{\Delta U_o} \cdot \frac{1}{8 \cdot f} \tag{3.20}$$

With an peak to peak inductance ripple $\Delta I_L = 300\,\text{mA}$ and a maximum ΔU_o of $\approx 0.01 \cdot U_o$ and the switching frequency f.

$$C_o \geq \frac{300\,\text{mA}}{0.01 \cdot 3.95\,\text{V}} \cdot \frac{255}{8 \cdot 200\,\text{MHz}} = 37.8\,\mu\text{F} \tag{3.21}$$

3.2.1. System Identification

The system used in this work is a step-down converter as shown in Figure 3.2a. The system is a clocked step-down converter, therefore it consists of two clocked circuits. Clocked circuits are not linear time-invariant because they change their behaviour by switching the File Effect Transistor (FET). Furthermore, the current of a buck converter can only be

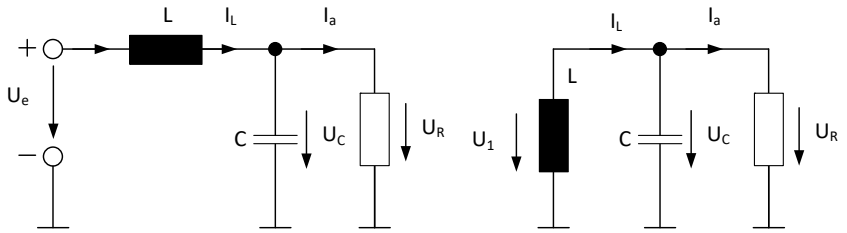


Figure 3.8: Simplified interval schematic of a buck converter, interval Td: left interval Td': right

controlled with a connected load. In this case, the load is an LED which is non-linear, too. Biolek et al. [149] and Tannir et al. [150] describe a model to average the two stages of the step-down converter to enable the controller design. The second approach to identify the system is to record the step response of the converter and to use the system identification toolbox of MATLAB®. Both transfer functions are compared at the end of this chapter. Middlebrook and Cuk [151] define the two stages of a buck converter (3.22) and (3.23).

$$\text{interval Td:} \qquad \dot{x} = A_1 x + b_1 u \tag{3.22}$$

$$\text{interval Td':} \qquad \dot{x} = A_2 x + b_2 u \tag{3.23}$$

The two simplified stages are shown in Figure 3.8. The change of the capacitor voltage U_C in both stages is described by using superimposition

$$\begin{aligned} U_C{}' &= U_R \\ U_R &= I_a \cdot R \\ I_a &= -C\frac{\mathrm{d}U_C{}'}{\mathrm{d}t} \\ \frac{\mathrm{d}U_C{}'}{\mathrm{d}t} &= -\frac{U_C{}'}{RC} \\ I_L &= C\frac{\mathrm{d}U_C{}''}{\mathrm{d}t} \\ \frac{\mathrm{d}U_C{}''}{\mathrm{d}t} &= \frac{I_L}{C} \\ \frac{\mathrm{d}U_C}{\mathrm{d}t} &= -\frac{U_C}{RC} + \frac{I_L}{C} \end{aligned} \tag{3.24}$$

The change of the inductor current I_L is described by

$$\text{interval Td:} \quad \frac{\mathrm{d}I_L}{\mathrm{d}t} = -\frac{U_C}{L} + \frac{U_e}{L} \tag{3.25}$$

$$\text{interval Td':} \quad \frac{\mathrm{d}I_L}{\mathrm{d}t} = -\frac{U_C}{L} \tag{3.26}$$

Resulting in a following state-space model

$$A1 = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \qquad b1 = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix} \tag{3.27}$$

$$A2 = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \qquad b2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.28}$$

Setting $u\,(t) = V_{in}\,(t)$ and using the average values of V_C and I_L the averaging model will result in:

$$x = \begin{bmatrix} V_C\,(t) \\ I_L\,(t) \end{bmatrix} \tag{3.29}$$

$$A_a = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \qquad b_a = \begin{bmatrix} 0 \\ \frac{D}{L} \end{bmatrix} \tag{3.30}$$

Where D is the duty cycle. In this case, the load is not a resistor as written in (3.27) and (3.28), it is an LED. The simple equivalent circuit of a diode is a resistor in series with a voltage source resulting in the schematic shown in Figure 3.9 The change of the capacitor voltage U_C can be described as

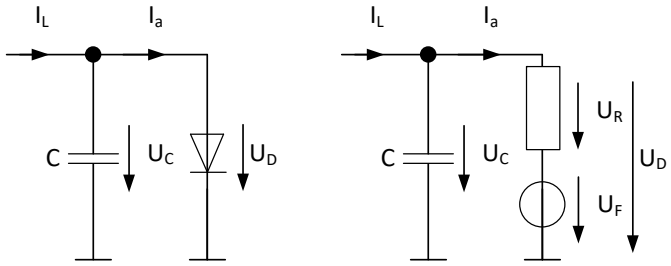


Figure 3.9: Load of the converter replaced by a diode (left) and equivalent circuit a resistor in series with a voltage source

$$
\begin{aligned}
U_C{}' &= U_R + U_F \\
U_R &= I_a \cdot R \\
I_a &= -C\frac{\mathrm{d}U_C{}'}{\mathrm{d}t} \\
\frac{\mathrm{d}U_C{}'}{\mathrm{d}t} &= -\frac{U_C{}'}{RC} - \frac{U_F}{RC} \\
I_L &= C\frac{\mathrm{d}U_C{}''}{\mathrm{d}t} \\
\frac{I_L}{C} &= \frac{\mathrm{d}U_C{}''}{\mathrm{d}t} \\
\frac{\mathrm{d}U_C}{\mathrm{d}t} &= -\frac{U_C}{RC} + \frac{U_F}{RC}
\end{aligned}
\tag{3.31}
$$

The state-space changes to

$$
A_a = \begin{bmatrix} -\frac{1}{RC} & \frac{1}{C} & \frac{1}{RC} \\ -\frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \qquad x = \begin{bmatrix} V_C(t) \\ I_L(t) \\ U_F \end{bmatrix} \tag{3.32}
$$

Determining the diode current I_D from of the capacitor voltage U_C the output matrix is defined as

$$
I_D = Cx + Du \qquad C = \begin{bmatrix} \frac{1}{R} & 0 & -\frac{1}{R} \end{bmatrix} \qquad D = 0 \tag{3.33}
$$

Using the measurement data from Section 2.4.2 will give the simple equivalent circuit values from the LED. The equivalent circuit of the LED at a

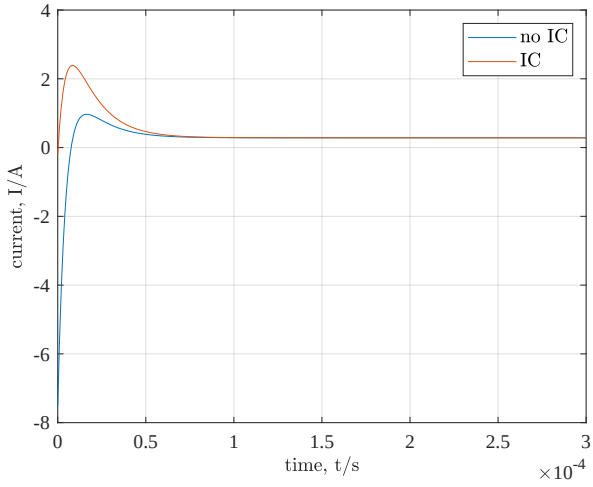


Figure 3.10: Step response of the average state-space system without initial condition and with the initial condition

temperature of 60 °C is (3.34)

$$U_F = 2.65\,\text{V} \qquad R = 0.352\,\Omega \tag{3.34}$$

To use the resulting state-space model of the system, it is necessary to adjust the initial values of the internal state x. The voltage of the equivalent circuit of the LED has to be set to its constant value of 2.65 V.

$$A_a = \begin{bmatrix} -284090 & 1 & 284090 \\ -147060 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \qquad b_a = \begin{bmatrix} 0 \\ 80883 \\ 0 \end{bmatrix} \tag{3.35}$$

$$C = \begin{bmatrix} 2.8409 & 0 & -2.8409 \end{bmatrix} \qquad x = \begin{bmatrix} V_C\,(t) \\ I_L\,(t) \\ 2.65\,\text{V} \end{bmatrix} \tag{3.36}$$

The step response of the average state-space system with the initial condition $x = \begin{matrix} 0 \\ 0 \\ 2.65\,\text{V} \end{matrix}$ is shown in Figure 3.10. It can be identified that the step response starts with a negative output. Reason for this are the initial conditions. The state-space model is only valid for output currents >0 A. Therefore, the internal capacitance voltage has to be greater-equal to the LED voltage source. To consider the entire system, the initial coil current has to be specified, too. Previous SPICE simulation results are used to

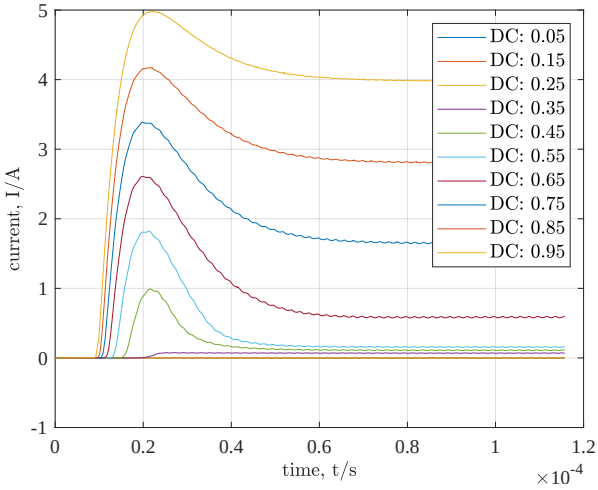


Figure 3.11: Step response of the system at different duty cycles of 0.05 to 0.95

identify the current which result in (3.37) of the initial state.

$$x = \begin{bmatrix} 2.58\,\text{V} \\ 3\,\text{A} \\ 2.65\,\text{V} \end{bmatrix} \tag{3.37}$$

The second line in Figure 3.10 is the step response with initial conditions provided by the SPICE simulation. The output current starts at 0 A and settles with an overshoot to 200 mA. The steady state output of both simulations is nearly the same. These information will lead to the fact, that the average state-space model cannot be used for the controller design because it is not possible to include the initial conditions in the bode plot for controller design. Therefore, another approach is needed to identify the system. By a step response, the system can also be identified and modelled. MATLAB® has included a controller design toolbox which can identify the plant for which the controller will be used. The toolbox can process a step response, an impulse response, a wide pulse response or arbitrary I/O data. All types of responses can be generated using the SPICE simulation. The step response of the system is already simulated and results are available, this is why it was used to identify the system. By adjusting the PWM duty cycles for different simulations, a list of step responses of the system can be plotted. Figure 3.11 shows the step response of the system at different duty cycles form 0.55 to 0.95. For all duty cycles lower than 0.45, the system does not work properly because the forward voltage of the LED

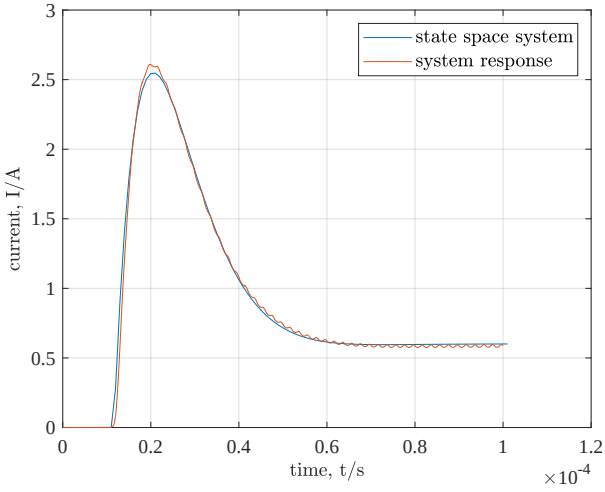


Figure 3.12: Step response of the identified state-space system compared to the SPICE step response with a duty cycle of 0.65

is not achieved. A duty cycle of 0.45 is the margin where the LED starts to conduct. The system has a PT2 like behaviour with an overshoot but the damping is near to 1. To identify a best fit system, the step response with a duty cyclic of 0.65 is used. The used LED has a maximum current of 1.5 A and therefore the duty cyclic of 0.65 with its steady state output of 0.7 A fits well in the operation area. The toolbox can use following target systems for the identification:

- one pole
- two real poles
- an underdamped pole pair
- an underdamped pole pair and a real pole
- a state-space model

The averaged system derived from the schematic has two states, the inductor current and the capacitance voltage. For this reason, the system is identified using a state-space model with two states, too. For the state-space model the plant order and an input delay can be defined. The identified state-space is shown below and the step response of the state-space model is shown in Figure 3.12. It can be identified, that the system (3.38, 3.39) fits the step responses of the SPICE simulation. This system can be

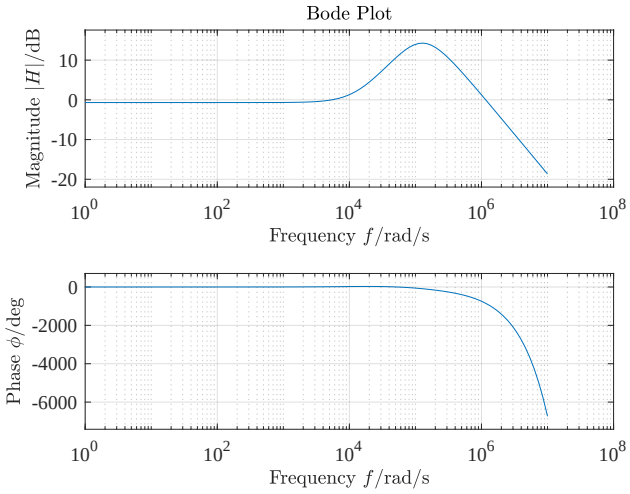


Figure 3.13: Bode diagram of the identified system for controller design

used for the controller design for the chosen step-down controller system.

$$A = \begin{bmatrix} -214320 & 82782 \\ -167110 & -12096 \end{bmatrix} \qquad B = \begin{bmatrix} -171 \\ -108.9853 \end{bmatrix} \tag{3.38}$$

$$C = \begin{bmatrix} -991.8706 & -45.3591 \end{bmatrix} \tag{3.39}$$

3.3. Controller Design

This section describes the LED current controller. The controller design is based on the identified system described in Chapter 3.2.1 using a state-space model. Figure 3.13 shows the bode plot of the identified system. The bode diagram identifies a PD behaviour. Therefore, a PI- or an I-controller can be used to control the system. The phase margin of the system is $-670°$ and the gain margin is 0.53 dB. This leads to the fact that the closed loop system is unstable. To increase the phase margin as well as the gain margin a PI-controller is appropriate. The I of the controller will result in no steady state error and adjusts the phase margin. The P can be used to adjust only the required phase margin. In the bode plot in Figure 3.13, the magnitude increases with a gradient of 20 dB per decade at approximately 8×10^3 rad s^{-1}. At approximately 128×10^3 rad s^{-1} the magnitude decreases with a gradient of -20 dB per decade. The resulting dome of the magnitude is the reason for the negative phase margin as well as the missing gain margin. To damp the dome of the magnitude, the Ki of the PI-controller is placed. A Ki decreases the magnitude with a

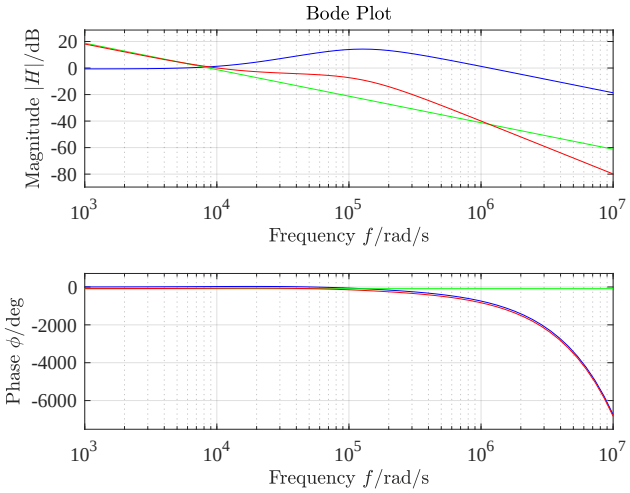


Figure 3.14: Bode diagram of the system (blue), controller (green) and the corrected system (red)

gradient of -20 dB per decade. By shifting the Ki, the 0 dB gain crossing frequency is shifted. The plant with the included Ki has a magnitude with a gradient of -20 dB per decade up to approximately 8×10^3 rad s^{-1}. It will be flat from 8×10^3 rad s^{-1} to 128×10^3 rad s^{-1} and will than start to decrease with a gradient of -40 dB per decade. Allowing a maximum phase margin and a gain margin, the Ki is placed at 8×10^3 rad s^{-1}. Figure 3.14 shows the bode plot of the system, the controller and the corrected system. Using this controller will change the phase margin to 113° and the gain margin to 9 dB which results in a stable and fast system. Therefore, it is not required to add the Kp of the controller. Previous results suggest that an I-controller is sufficient for the system. Using only an I-controller will also reduce the implementation effort of the controller. In Figure 3.15 the step response of the close system is shown. The system is stable, has no steady state error and is fast. With a system settle time of approximately 1 µs, the controller is fast enough to be used for a LED driver. The controller is included into the SPICE simulation of the step-down controller to evaluate the designed controller. Simulation results are also shown in Figure 3.15 in red. It can be observed that the system identified by MATLAB® does not consider the input delay of the system. Nevertheless, the step responses are similar and the output current of the controller is fast and reaches steady state output. Furthermore, the controller works fine in the MATLAB® simulation as well as in the SPICE simulation. The current rises in 1 ms up to the set point of 1 A.

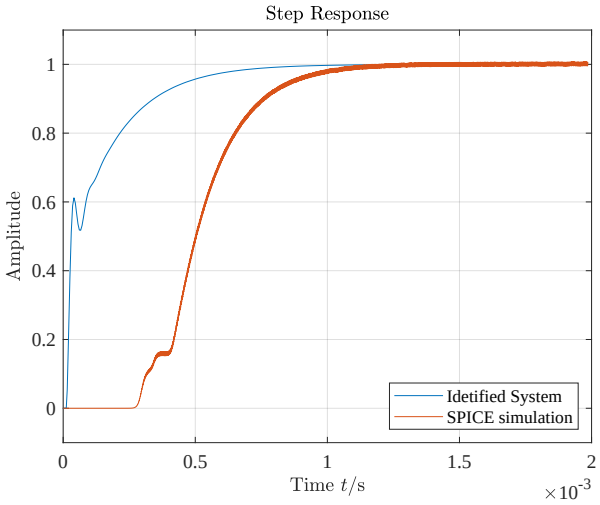


Figure 3.15: Step response of the corrected closed loop system LED current driver simulated with the model (blue) and simulated in SPICE (red)

3.4. Summary

This chapter describes methods to drive LEDs and analyses the advantages and disadvantages of the possible methods. Due to their steep characteristic curve, LEDs need to be supplied by constant DC forward currents. Beside constant current sources, LEDs can also be driven at their maximum current and the light intensity can be reduced by pulsing the maximum current. LEDs can be driven using different methods; linear, step and new approaches. Classic and up-to-date drivers are introduced taking important values of drivers into account. Part of the up-to-date drivers are inductor less approaches reducing the size of the driver and allowing a full integrable design with less external devices. As the step-down converter was identified as an LED driver with a high efficiency and a relative simple design, it was chosen to be used in this work. To use the step-down converter combined with a thermal management, a current controller was designed. As a basic step to design a controller, the system behaviour needs to be modelled to simplify the controller design. The step converter uses a clocked switch whereby the system can be described by two states with two different schematics. This impedes to map the system into a single function. Therefore, the identification was performed by building an average model of the step converter where the two schematics are converter into the state-space model and are averaged using an averaging factor. In the second approach for system modelling, the MATLAB® system iden-

tification toolbox was used. MATLAB® analyses the step response of the open loop system and estimates a state-space model of the system for the predefined plant order. The resulting state-space system has a well fitting step response compared to the simulation results from SPICE. The controller can be designed using the system behaviour in the state-space model. By plotting the bode diagram and analysing the system behaviour an I-controller was identified as the best controller behaviour for the system. For the step response behaviour in MATLAB®, an I-controller with approximately $8 \times 10^3\,\mathrm{rad\,s^{-1}}$ gives very good results. The current rises in less than 1 ms and in is steady state at 1 A. Including the I-controller into the SPICE simulation results in a slightly slower step response with a rising time of 1.25 ms and steady state as well.

4

Discrete Component Test System

What I mean is that if you really want
to understand something, the best way is to try and
explain it to someone else.
That forces you to sort it out in your own mind.

Douglas Adams

This chapter describes the development of a discrete system which tests the desired hardware system, the digital code including current controller, temperature determination, thermal management and communication via Universal Asynchronous Receiver Transmitter (UART) interface. The overall objective of this work is the development of an ASIC, therefore the discrete system is designed to reuse most of the components for the ASIC design. The digital part of an ASIC can be synthesised from a Hardware Description Language (HDL), such as Very High Speed Integrated Circuit Hardware Description Language (VHDL) or verilog HDL. Therefore, the controller and thermal determination as well as thermal management is implemented by using VHDL. As part of the design, the step-down converter which was used to control a constant current for the LED, will be used in the discrete as well as in the integrated design. The step-down controller for the constant current supply of the LED is based on the description in Chapter 3. A simplified block digram of the desired discrete design is shown in Figure 4.1. In the discrete design, the VHDL code developed for the ASIC design is tested in an FPGA. The current can be specified by a device connected to the UART interface. The current and the voltage of the LED have to be measured, digitised and transferred to the FPGA. The measured current is needed to control the LED as well as to determine the LED temperature using the forward voltage method. The FPGA

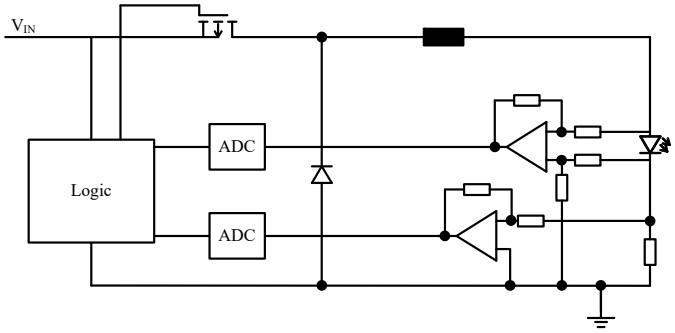


Figure 4.1: Block diagram of the proposed discrete system with step-down convert, current and voltage measurement and logic for current and LED control

measures the LED current using a shunt resistor and a current monitor from Texas Instruments (TI). By adjusting the PWM input of the step-down controller, a constant current is applied to the LED. In parallel the LED voltage has to be measured because it needs to determine the LED temperature. For each measurement an amplifier processes the signal before digitalisation. This is needed to map the measurement to the ADC reference voltage which maximises the digital resolution of the signal. Results of the system identification from Chapter 3 are used to determine the ADC conversion speed. The physics of the step-down converter with included controller allow a maximum current increase of 11.2 A ms^{-1}. When a ADC with 8 bit is used to measure currents from 0 A to 1.5 A, the maximum resolution is 5.88 mA bit^{-1}. To detect changes of 5.88 mA, the ADC must have a minimum conversion rate of 2 kHz.

4.1. Hardware Setup

Using a development board to test the discrete design reduces the development effort. Supply, peripherals as well as I/O and communication are ready to use. A suitable FPGA development board is the Atlys™Spartan-6 FPGA board from Digilent®. The Atlys™circuit board, shown in Figure 4.2, is a complete, ready-to-use digital circuit development platform based on a Xilinx® Spartan®-6 LX45 FPGA. The on-board collection of high-end peripherals, including Gbit Ethernet, High Definition Multimedia Interface (HDMI) Video, 128MB DDR2 memory array, audio and USB ports make the Atlys board an ideal host for complete digital systems built around embedded processors, such as Xilinx's MicroBlaze™.

Atlys is fully compatible with all Xilinx® CAD tools, including ChipScope™, EDK, and the free WebPACK™, thus designs can be completed

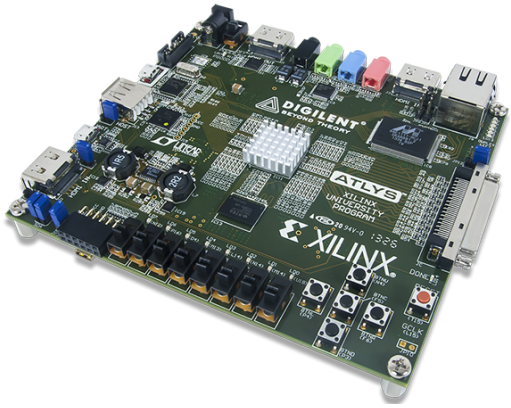


Figure 4.2: Atlys Spartan-6 FPGA Trainer Board by DIGILENT [152] used for the digital part of the system

with no extra costs [152]. A high speed Vmod Very High Density Cable Interconnect (VHDCI) connector allows the connection of extension boards. Digilent® provides several extension boards, e.g. stereo camera board or touch screen board. For this project, a custom extension board has to be developed containing all discrete elements needed for the LED driver and thermal management. These parts are the step-down converter including the LED and the measurement circuits for LED voltage and current. The step-down converter schematics are shown in Figure 3.2a. Parts of the step-down converter are used corresponding to the design in Chapter 3.2 with an inductance of 6.8 µH and a capacitance of 100 µF. Both current and voltage measurements are performed by the ADC08060 ADC from Texas Instruments. The ADC08060 has a resolution of 8 bit and can be used with a sample time of up to 80 Mega Sample Per Second (MSPS). Each ADC has two reference voltage inputs, one for the minimum reference voltage and one for the maximum reference voltage. Initially, the lower reference voltage is defined to 0.304 V and the upper reference voltage is set to 1.9 V for both ADCs. Later, these values are adjusted to the corresponding maximum and minimum output voltages of the pre-processing. This results in a maximum used ADC range. The output of the ADCs is connected in parallel by the high speed VHDCI connector to the FPGA. The current is measured by a 0.02 Ω shunt resistor. Current and voltage need to be pre-processed before they can be digitised using the ADC. A resulting maximum drop voltage across the resistor of 0.04 V needs to be amplified to achieve a valid conversion result. For this purpose, the INA214 from Texas Instruments is a suitable amplifier. It is a special current sense amplifier available in six different fixed gain factors 50 V/V, 100 V/V,

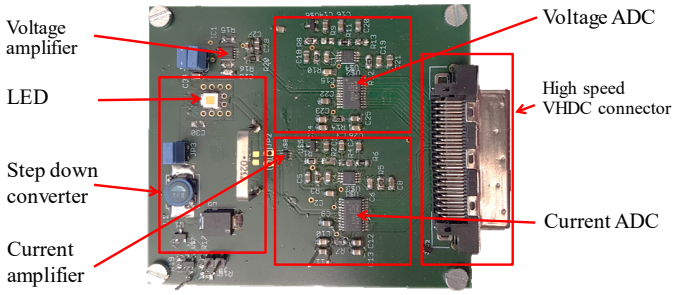


Figure 4.3: Extension board for the Atlys board including LED, step-down converter, and measurements for LED current and voltage

75 V/V, 200 V/V, 500 V/V and 1000 V/V. For the conditions applied in this work, the gain of 100 V/V is applicable resulting in an output voltage of 0 V to 3 V. The forward voltage is processed by an instrumentation amplifier the INA326. By applying an external resistance of 400 kΩ to the gain set inputs, the internal gain of the UNA214 is configured to 0.5 resulting in an output voltage of 1.475 V to 1.625 V[88]. The resulting extension PCB is given in Figure 4.3. The board layout as well as the schematic of the extension PCB are shown in Appendix B in Figure B.1 and Figure B.2 respectively.

4.2. Discrete Implementation

The combination of Atlys board and extension board results in a finished discrete system. Several test points are available to test and measure system behaviour and functionality. The software has to be developed with a finished hardware. Tasks of the software are controlling the LED current and determining the current LED temperature. Furthermore, a communication interface is needed to transfer current set points to the discrete system and to receive the current temperature of the LED. The communication interface uses the USB-UART FTDI chip available on the Atlys board. To conclude the functionality, the DTM needs to be implemented in an efficient way.

4.2.1. Integrated Current Controller

The integrated controller is designed in VHDL. The advantage of using VHDL as programming language is that it can be used to configure a reconfigurable hardware device and can be used to synthesise hardware designs for an ASIC. It is based on a 16 bit fix-point PID controller and is first simulated to ensure right behaviour. SPICE does not allow to simulate the

controller with digitizes measured voltage and current. Controller design and test can be easily implemented in MATLAB® Simulink®. It also has a plug in called Simscape® with the Open Electrical library. MATLAB® Simscape™allows to simulate electrical circuits embedded to Simulink®. Therefore, the simulation of the step-down convert with LED as load was rebuilt in MATLAB® Simscape™. All values of the designed step-down converter were kept equal to the SPICE simulation. Since it is not possible to include custom parts as in spice, the LED was replaced by a standard diode. The coefficients of the standard diode were adapted to the values given in the data sheet of the LED and the SPICE custom LED used for the simulation in Chapter 3.

The controller will be used in a digital FPGA. Analogue current measurements as reference for the controller have to be convected to digital values which is also implemented in the controller circuit in Simulink®. Output of the digital controller of the FPGA is a PWM, driving the switching transistor of the step-down converter. Even the step width of the PWM is modeled in Simulink®. The forward current of the LED is measured by a shunt resistor converting the current into a voltage by Ohm's law. The voltage is acquired by a differential amplifier and digitised by an 8 bit ADC. The shunt resistor is included in the circuit of the simulation, the relation between voltage and ADC value is modelled by a linear equation and rounded to integers. The transfer function of the ADC was identified by the reference voltages and the number of bits. Combining the amplifier with the ADC results in an approximate linear function (4.2).

$$I_{ADC} = V_{0.02} \cdot P_{INA214} \cdot m_{ADC} - b_{ADC} \tag{4.1}$$

$$I_{ADC} = V_{0.02} \cdot 50 \cdot 245 - 48 \tag{4.2}$$

Where I_{ADC} is the digital 8 bit value, $V_{0.02}$ is the voltage across the current measure shunt, P_{INA214} is the amplification of the current sense amplifier, m_{ADC} is the slope of the ADC function and b_{ADC} is the intercept of the ADC function. P_{INA214} is taken from the device description, m_{ADC} and b_{ADC} are identified by measurements. The internal limit of the calculated error is also taken into account and limited to 255. Due to the fact that the controller is a pure I controller, the set point value is defined as an 8 bit value corresponding to the values from the ADC. As the controller will be implemented in an FPGA, the maximum clock rate of the FPGA determines a PWM resolution of 8 bit, too. To include the step-width in the simulation, the output of the I-controller is rounded and the PWM output is mapped to the 255 steps available by the 8 bit counter for the PWM.

The PWM input signal is a signal between 0 V to 5 V for the system identification design. In this system, the PWM input signal has a rage of 0 to 1. Therefore, the Ki was identified in Chapter 3.3 as part of the controller and must be divided by 5 to avoid instability. A good controller design

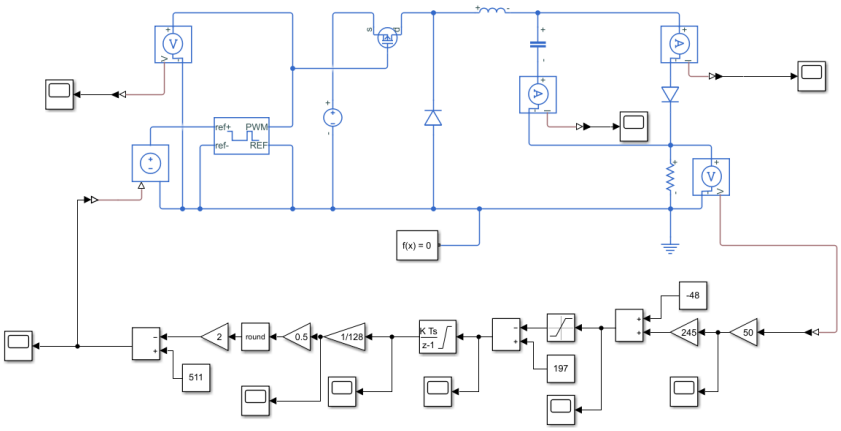
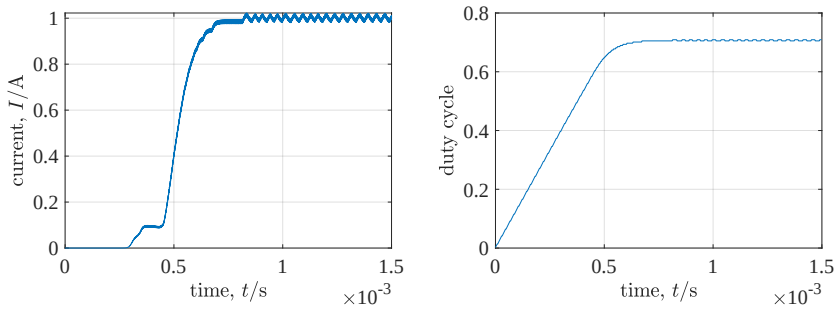


Figure 4.4: Simulation model of the step-down converter with current ADC approximation, controller, value limitation to the digital number and digitisation of PWM

was detected using a division factor of 10 resulting in a Ki of 800 because an overshoot was detected using a division factor of 5. Figure 4.4 depicts the resulting simulation structure. The set point in Figure 4.4 is defined as 197 because this value represents 1 A using the transfer function of the ADC. The clock speed of the FPGA is 100 MHz, this clock is used to count upwards and the 8^{th} bit is used as the clock bit for the controller, which divided the clock speed by 2^{10} resulting in a controller frequency of 97.66 kHz. When the controller integrates the error input value in each step, a controller with a $Ki = 97.66e3$ will be built. To reach a Ki of ≈800, a divisor of 122 is needed. Divisions in VHDL and in an FPGA or an ASIC are complex to perform. Conversely, shifting bits is an easy way to replace divisions. By shifting bits, values can be easily divided by a factor based on 2. The next matching divisor based on 2 is 128 resulting in an Ki of 762.9. In Figure 4.4, the deviser of 128 is already included and placed between the discrete integrator and the PWM generator. Figure 4.5 indicates the simulated step response and the duty cycle of the PWM. As shown in Figure 4.5a, the LED current reaches steady state current of 1 A after ≈0.7 ms. The output current starts to swing after 0.8 ms with an amplitude of ±20 mA, this is related to the relatively low step-width of the PWM of 256 steps. When the desired current falls between two step-width of the PWM, the current cannot reach its set point and will swing between the two possible currents. This can also be reflected in Figure 4.5b, where the duty cycle of the PWM is shown.

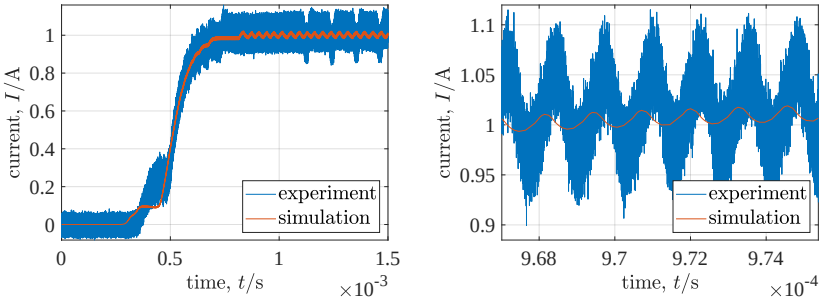
After applying a unity step to the input of the controller, the duty cycle of the PWM rises from 0 to 0.7051 and subsequently starts to change to 0.709 and back to 0.7051 periodically. The difference between both steps



(a) (b)

Figure 4.5: Simulation results using Simscape to simulate the step response of the step-down converter with digital controller and 8 bit PWM(a) and the duty cycle of the PWM (b)

is 3.9×10^{-3} what is approximately $1/255$ and the step width of the PWM. After the finished tests and simulations of the integrable controller, the design is implemented into the FPGA on the Atlys board. After implementing the code using Xilinx ISE tools, the discrete system with current controller is tested and validated. Same as in the simulation, the set point is defined in an 8 bit format and transmitted to the FPGA via the UART interface. To transmit 8 bit, the UART interface is used in the 8N1 configuration. 8 represents 8 bit of data, the N represents no parity bit and the 1 at the end represents one stop bit. The speed of the UART is configured to 115 200 bit s^{-1}. A 197 is transmitted via the UART interface to the Atlys board to achieve a step response of 1 A. The step response is measured by a Agilent MSO9404A Mixed Signal Oscilloscope with 4 GHz, 4 Analogue and 16 Digital Channels. N2820A/21A High-Sensitivity High Dynamic Range Current Probe is used to measure the forward current of the LED and a standard probe is connected to the PWM output of the FPGA. The step response of the experiment is compared to the simulation in Figure 4.6a. The measured signal is noisy but it is steady state and has the same forward current as in the simulation. Comparing the settle behaviour of simulation and experiment, they nearly fit each other exactly. The settle time for the discrete system is ≈0.8 ms and the system starts to swing with the same amplitude after reaching steady state. For a better comparison, the steady state region of the step response is zoomed in and shown in Figure 4.6b. Compared to the current ripple of the simulation, the steady state current ripple is slightly bigger in the experiment. Amplitude of the current ripple in the simulation result is ±10 mA, in the experiment it has an amplitude of ±40 mA. Variations in the discrete elements can be one reason for the difference of ±30 mA. Furthermore, the wires of the circuit



(a) (b)

Figure 4.6: Step response of the step-down converter with digital controller implemented in the FPGA with simulated step response with discrete step response (a) and zoomed ripple of experiment and simulation (b)

Table 4.1: Settle time of the integrated current controller for different forward currents

Current	8 bit value	Settle time	Steady state
1.0 A	197	0.8 ms	yes
0.9 A	160	0.8 ms	yes
0.8 A	135	0.9 ms	yes
0.7 A	110	0.9 ms	yes
0.6 A	90	1 ms	yes
0.5 A	66	1 ms	yes
0.4 A	43	1.45 ms	yes
0.3 A	24	1.8 ms	yes
0.2 A	1	2 ms	yes
0.1 A	-	-	-

and the interference of the PWM to the wires on the PCB are not simulated.

For validating the system, input steps in the rage of 0.1 A to 0.9 A are applied and the resulting step responses are checked in terms of settle time and steady state current of the controller. The values for each current are listed in Table 4.1. This table shows, that the current controller works in a fast and stable way. A relatively constant current is achieved at the LED and can be adjusted over the entire operating range. Current set points can be transmitted using the UART interface. Hence, it is possible to activate the LED in different luminosities.

Table 4.2: Xilinx ISE used cells by design summary report showing the used resources by each of the three different temperature determination methods

	linear	quadratic	pulsed
Registers	346	446	219
LUTs	416	598	165

4.2.2. Temperature Estimation

In the discrete system, the FPGA should be able to identify the temperature of the LED. For the internal temperature estimation, the forward voltage method described in Section 2.4.1 is used. Each of the three possible variations of the forward voltage is implemented in VHDL and the used registers and Look Up Tables (LUTs) by the variation are compared for the identification of the optimal implementation of temperature determination. Values used in the forward voltage method, forward and current, are available in 8 bit values from the ADC. To reduce the calculation effort internally, the forward voltage coefficients for intercept and slope are mapped to the 8 bit values from the ADC. The characteristic curves identified by the calibration described in Section 2.4.2 are adapted to fit the voltages received by the ADC as specified for the set point used in the integrated controller design in Section 4.2.1. Intercept and slopes of (2.12) depend on the forward current. To reduce the number of used constants in the FPGA, 10 slopes and intercept pairs are predefined in VHDL. Each slope and intercept pair is related to a fixed forward current: 0.1 A, 0.2 A, 0.3 A, 0.4 A, 0.5 A, 0.6 A, 0.7 A, 0.8 A, 0.9 A and 1 A. The predefined pairs are calibrated by an experiment of the CREE® XLamp® LED, if another LED is connected and supplied, the parameters can be adopted using the UART interface. If a 254 is transmitted to the FPGA, it will change into configuration mode. In this mode, new parameters for the temperature estimation can be transferred. Slope and intercept values are stored in an 11 bit vector each. Each new slope and intercept value has to be divided into two 8 bit vectors resulting in an amount of 36 8 bit vectors which have to be transferred to adapt the temperature determination. Which slope and intercept pair is used to calculate the temperature of the LED is determined by using the actual value of the forward current measured by the current ADC. Each pair has a defined validity range. For example, the slope pair defined for 500 mA is valid from 450 mA to 550 mA; from 550 mA to 650 mA the slope and intercept pair of 600 mA is valid. The steps are defined in a state machine controlled by the actual value of the forward current.

The same procedure is used for the quadratic approach and the stepped approach. Table 4.2 lists information about the used cells in the Spartan 6 FPGA for each approach. It can be seen that PJTM uses the smallest amount

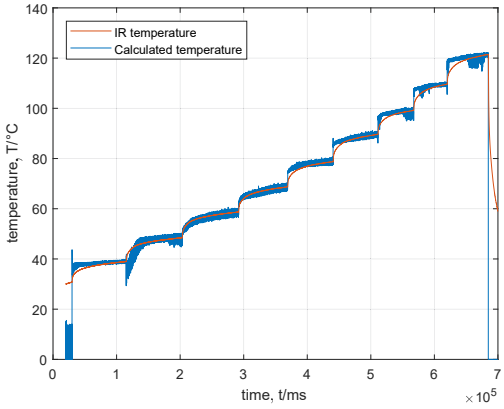


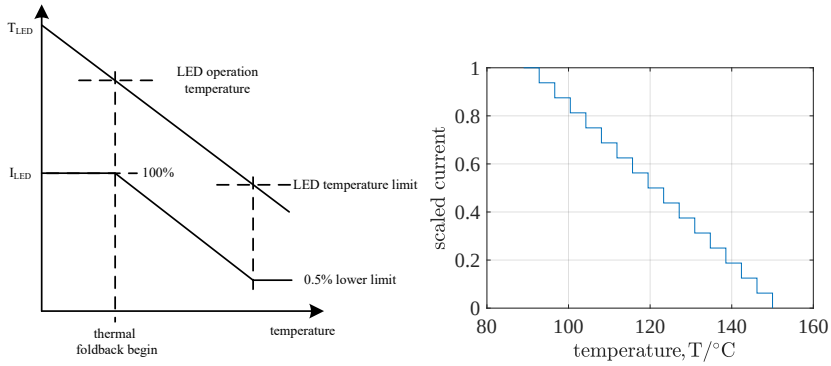
Figure 4.7: Received LED temperature from the FPGA and measured temperature of the IR-camera to validate the internal temperature determination. Forward current is increased successive by 100 mA.

of registers and LUT. Followed by the linear approximation of the forward voltage method. Most resources of the FPGA are used by the quadratic approach, here more than double the amount of LUT and registers are needed compared to the PJTM approach. To store the temperature internally a signed 8 bit variable is used. Therefore, the temperature can range from −256 °C to 255 °C. For validation of the temperature determination, current internal temperature values are transmitted via the UART interface and received by a computer. If the current controller is turned off, no temperature estimation is possible and the FPGA transmits 0 °C. After a synthesis and implementation of the designs, each approach is written into the FPGA for a device configuration on the Atlys board and tested with the LED. To verify the temperatures measured by the FPGA, the surface temperature of the LED is measured additionally by an IR camera used in Chapter 2.5.2. Figure 4.7 illustrates the internal determined LED temperature and the temperature measured by the IR-camera. The forward current of the LED is increased successively by 100 mA in a range of 0.1 A to 1 A in this test. The steady state temperatures determined by the forward voltage method fit the temperatures captured by the IR-camera well. Comparing the regions where the forward current is increased, it can be established that the internal temperature determination works faster than the IR-camera. It takes time until the surface of the LED heats up. The internal temperature determination directly measures the temperature of the junction of the LED. As depicted, good results can be achieved at the operation point. The determined temperatures fit the Infrared (IR) camera temperatures very well. The maximum error of this approach for temperature calculation is ±3 °C.

These results can only be achieved when the LED is operated in a known environment. Compared to the linear approach, the quadratic approach gives an error of ±3 °C even when the LED is not operated in the operation point. Therefore, it can be operated at a wider operation range (currents like 0.1 A to 1 A and temperatures from 20 °C to 110 °C). The PJTM results in slightly lower identified temperatures compared to the IR camera temperatures −5 °C to −3 °C. This effect can be explained by the cooling effect of the reduced current used to measure the temperature. Furthermore, the TTE and the pulse current effect described in Section 2.4.2 are possible reasons for this effect [76]. Since a pulsed approach is used for the temperature determination, the temperatures cannot be detected constantly. For the example, shown in Figure 2.13, the LED is driven with an operation current of 10 s and subsequently the temperature is measured within the 10 ms time frame. Between the measured pulses, the temperature of the junction of the LED is unknown and steep temperature changes cannot be detected.

4.3. Integrated Thermal Management

The integrated thermal management is also first tested with the discrete design. It is based on the considerations of Chapter 2.7. As a main objective of the thermal management, the maximum operation temperature of the LED should not be exceeded. The data sheet of the LED defines this maximum LED temperature. For the CREE® XLamp® LED it is defined as 150 °C [88]. It is essential to prevent such temperatures or temperatures beyond this value. Therefore, a management theory is developed which reduces the forward current in case of temperatures rising beyond the maximum temperature. Based on the DTM introduced in Chapter 2.7, a temperature controller is developed to be included into the LED driver. Similar to the design of Zha et al. [138], Texas Instruments [139] the three-stage solution, which was introduced in Chapter 2.7.5, is used. A detailed functionality information of the DTM used by Texas Instruments is shown in Figure 4.8a. As long as the temperature of the LED is lower than its standard operation temperature (stage S_1), the LED is supplied with its desired current. This current must be in the operation conditions of the LED. When the LED temperature exceeds the standard operation temperature, the forward current is scaled proportionally (stage S_2). The LED is set into power-off or minimum current mode, in this case ≈0.5 %, if the temperature exceeds the maximum operation temperature (stage S_3). For the implemented DTM, the three states are defined for the used LED type, the CREE® XLamp®. In stage S_1, the LED is supplied with the designed current transmitted via the UART interface. In stage S_3, the LED is in power down mode to prevent damages while the LED is overheated. For a later implementation in the ASIC, the design should be as compact



(a) (b)

Figure 4.8: Proposed thermal management by Zha et al. [138], Texas Instruments [139] (a) and the here implemented management using a stair function of 16 stairs to reduce the size of the ASIC (b)

as possible using minimum number of transistors by full functionality. The here used Spartan 6 has internal multipliers which can be used for the proportional scaling, but in the ASIC the multipliers have to be created out of Complementary Metal Oxide Semiconductor (CMOS) technologies. Multipliers generated from standard cells will need a high amount of resources, i.e. number of transistors. This will increase the size of the ASIC. By changing a linear current reduction to a stepped function, no divider is needed. Steps can be calculated using addition, subtraction and bit shifting. Adders and bit shifters are easy to generate and do not need as much space as multipliers. Therefore, stage S_2 is divided into 16 steps and the forward current is reduced by 1/16 in each step until stage S_3 is reached. Using this mathematics the DTM is implemented as following: in the first of the 16 steps, from 89 °C to 93 °C, the current set point is shifted by 4 bit. The results are subtracted from the initial set point resulting in a set point of 15/16. This methodology is performed for each region 93 °C to 97 °C, 97 °C to 101 °C, 101 °C to 105 °C, 105 °C to 109 °C, 109 °C to 113 °C, 113 °C to 117 °C, 117 °C to 121 °C, 121 °C to 125 °C, 125 °C to 129 °C, 129 °C to 133 °C, 133 °C to 137 °C, 137 °C to 141 °C, 141 °C to 145 °C, 145 °C to 150 °C and above 150 °C. This results in a stair function shown in Figure 4.8b. With this functionality, the LED is turned off completely when state S_3 is reached. Subsequently, an external reset is needed to reactivate the driver and switch back from thermal shutdown. To overcome this external reset, two other exit methods for stage S_3 were implemented. PJTM can also be used as a possible exit strategy from stage S_3. As soon as the DTM reaches state S_3, the LED forward current is deac-

tivated completely. To determine the temperature of the LED, a low short supply current pulse is generated. As soon as the temperature of the LED drops under the threshold temperature for state S_3, the DTM changes back into state S_2. The second implemented exit strategy is to hold the LED active in state S_3 with the minimum current needed for the forward voltage method. The current is 200 mA because the step-down converter cannot provide a lower current for the LED. At this supply current the LED is still active and heats itself up. Therefore, the PJTM is the best fit exit strategy. To validate the DTM, the temperature of the LED is again measured by the IR-camera. Two tests are performed. In the first test the LED is supplied with the maximum current without DTM to get the reference temperature of the LED. The results of the first test are similar to the behaviour detected in Chapter 2.4.2. The LED heats up to a temperature above 160 °C. When the LED is cooled down, a second test is performed. In this test the DTM is active and the LED temperature does not exceed 120 °C. To analyse the dynamic behaviour, an external heat sink with fan is connected to the LED. First, the LED forward current is set to maximum. By the active DTM, the forward current is reduced to avoid overheating. After activating the fan attached to the heat sink, the forward current of the LED rises again. Dependent on the speed of the fan and the so created laminar flow, a better heat flux is achieved and the LED is cooled down while the current rises. As already mentioned in Chapter 2.7.5, the DTM cannot reach state S_3 without an external heat source. To test whether the thermal shutdown (S_3) works and if the exit method is also working, a hot air gun is used to heat up the LED. The thermal shutdown works well and with the implemented pulsed exit method the DTM changes back into state S_2 when the hot air gun is deactivated. Compared to the pulsed exit strategy, the LED heats further when supplied by the slowest possible current. Therefore, the pulsed strategy is the best fit strategy to prevent the LED from further thermal damage.

4.4. Summary

In this chapter, a discrete system was designed to test the previously developed methods in experiments. The discrete design includes the current controller for the LED and the measurement system for current and voltage measurement of the LED. Furthermore, it is possible to implement the forward voltage method in the three variations described in Chapter 2.4.2. To allow this functionality and keep the later ASIC design in mind, an FPGA development board from Digilent® was used because the VHDL code developed for the FPGA could be used later for the ASIC design. Part of the development board is an FPGA and its peripheral with communication interfaces. The step-down converter as well as the current and voltage measurement system were placed on an extension board. Parts of the step-

down converter were used correspondingly to the design in Chapter 3.2, an inductance of 6.8 µH and a capacitance of 100 µF. Current set points can be transmitted via an UART interface from a computer or microcontroller. Both current and voltage measurements are performed by an 8 bit ADC with a pre amplification. Because 8 bit ADCs are used, the results from the calibration of Chapter 2.4.2 were adapted to fit the 8 bit values, this reduces the calculation effort in the FPGA. The complete discrete system was simulated using the MATLAB® Simulink® plugin Simscape® and the Open Electrical library. This simulation environment allows to simulate the entire system including the amplifiers, ADCs and the internal controller. The simulation results lead to a changed controller because the ADC values are used for the internal current set point. Step response of the simulation has a settle time of ≈0.7 ms with a current ripple of ±20 mA evoked by the step-down converter ripple and the resolution of the PWM. After good results were achieved in the simulation, the current controller was implemented in hardware. Experimental step response of the discrete system fits the simulation results very well except measured noise. Furthermore, a test for different currents from 0.1 A to 1 A is performed analysing the settle time of the current controller as well as the steady state current. With the working current controller, the temperature estimation was implemented into the FPGA. All three variations are implemented and compared in terms of used registers and LUTs. As most constants and more multipliers are needed, the quadratic approach is the one using most resources of the FPGA with 446 registers and 598 LUTs. The pulsed approach uses approximately half of the resources needed for the quadratic with 219 registers and 165 LUTs because only one linear approximation has to be stored in the FPGA. In the middle region of resource usage, the linear approach can be designed using 246 registers and 416 LUTs. The pulsed approach has other drawbacks with regard to the lifetime of LEDs. Hence, the linear approach was identified as best fit for the design if the linearisation is performed in the operation area of the LED. With included thermal determination in the FPGA, the current determined temperature is constantly transmitted through the UART interface. In an experimental test, the internal determined temperature was compared to the surface temperature of the phosphor of the LED acquired by an IR-camera. The current is increased by steps from 0.2 A to 1 A and the temperatures are compared to the forward voltage approach. The results of the experiment show that the internal determined temperature of the LED rises faster compared to the external temperature which can be related to the thermal low-pass behaviour of the LED structure. Both the determined steady state temperature and the measured steady state temperature fit well. For the pulsed method, the PJTM, the temperature of the LED cannot be detected between the measurement pulses which could lead to overheating if the measure interval is defined as too low.

For the linear and the quadratic approach, the functionality and accuracy of the internal temperature determination using the forward voltage method determination was proven. With a working temperature determination which is essential for a thermal management, the DTM was included in the discrete design. From various thermal management techniques, an applicable version for LEDs was adopted and implemented in a resource efficient way. A three stage thermal management is used where in stage S_1 the LED is operated in standard mode with a defined constant forward current. In stage S_2, when the LED temperature exceeds its operation temperature, the forward current is reduced successively until the maximum temperature of the LED is reached. The behaviour was tested and the LED supply current reduces automatically when the LED heats up subsequently resulting in a current temperature balance without overheating the LED. Stage S_3 cannot be reached with the active DTM by the LED itself, therefore a hot air gun was used to further heat the LED. When the maximum temperature is reached, the DTM changes in state S_3 (thermal shutdown) where the LED operation is turned off completely. No temperature determination is possible while the LED is not supplied, an external reset is needed to restart the LED driver and supply the LED again. Two exit methods for the thermal shutdown where implemented and tested. The first uses an PJTM where the LED is supplied with short current pulses to determine the temperature and if it falls below the threshold of S_3 again, the DTM starts working in S_2. Another method is to turn into a low forward current mode where nearly no self heating occurs. In this mode, the LED temperature can be determined continuously and the DTM works in all stages. It can switch back into S_2, if the temperature falls again. By the tests the PJTM was identified as the best fitting approach to exit the thermal shutdown because low forward current mode still heats up the LED and can result in damage or life time reduction. All functionalities were implemented in VHDL to allow using it in the ASIC.

5

Design Of An ASIC Including LED Driver With DTM

There are of course many problems connected with life, of which some of the most popular are Why are people born? Why do they die? Why do they want to spend so much of the intervening time wearing digital watches?

Douglas Adams

As the usage of LED technology is increasing in lighting applications, the demand of LED drivers rises. The large amount of produced drivers results in a change from a discrete driver design to an integrated driver design. Higher design and development costs for the integrated LED driver can be split on the high number of devices. This fact results in a high amount of available integrated LED drivers. The previously designed discrete driver setup described in Chapter 4 needs to be implemented into an Application-Specific Integrated Circuit (ASIC). ASICs can be developed using different development tools available on the market. This chapter will introduce currently available development tools and show which tool is used in this work. For the implementation, a high number of manufacturing processes are available providing different Process Design Kits (PDKs) with standard cells. After selecting an appropriate software tool, a PDK has to be chosen fitting to the project and the software tools. This project is developed using the EUROPRACTICE IC Service. ”Europractice is an EC initiative which aims to stimulate the wider adoption of state of the art microelectronics and electronic system design methodologies and technologies within Europe and a wide range of modern design methodologies for IC, Photonics, MEMS, FPGA and Systems, for non-commercial

research and teaching are available to Academic Institutions and publicly funded Research Laboratories in Europe and some other countries where bilateral agreements are in place. Europractice membership and access to design tools is managed by STFC at the Microelectronics Support Centre, Rutherford Appleton Laboratory, UK."[153] The here used software tool and PDK has to be part of the Europractice family. After identifying the software tool and PDK, the Austria Mixed Signal (AMS) design flow is shown. Based on this design flow, the discrete design is transferred into an ASIC. First, the analogue part consisting of current and voltage measurement is implemented in a full custom analogue design. Afterwards the VHDL implementation of the FPGA is adapted to be synthesised in the chosen technology. Both designs, the analogue and the digital one are connected parallel and wired on chip level. After finishing the design by including the I/O ring, it is fabricated and packed. A test PCB is developed providing the needed external signals and the step-down converter as well as the LED. Finally, the complete design is tested and the test results are compared to the simulations and measurement results from the discrete implementation.

5.1. Design Methodology For LED Driver Integration

The design methodology for AMS designs is divided into two parts: the analogue implementation process and the digital implementation process. Both implementation processes are combined in one floorplan describing the positions of the the two subsystems on the chip. Part of the floorplan is also the interface between the two implementations. The design of AMS integrated circuits is extremely complex [154]. Especially the design of digital integrated circuits is so complex that design tools have to be used. These design tools are also extremely complex. It is essential to identify a combination of design tools which create a "tool path" for the individual project. Several design tools are available on the market and suitable design tools must be identified to develop the LED driver ASIC.

5.1.1. Software Tools

Several software tools are available for a CMOS ASIC development. This section gives an overview of available tools. Different work flows for mixed-signal systems are defined and the tools are evaluated by their functionality and support of the flows. The development of the LED drivers can be divided into two parts. The first part is the analogue part which is responsible for measuring and acquiring the forward voltage and the forward current of the LED. The second part is the digital part which consists of the current controller, temperature determination and the DTM. For the

mixed-signal design flow, four main strategies are common. The application of one of the four strategies depends on the relative size of the digital and analogue part. It is important to identify the size of the digital and the analogue part previously. For a design with a small analogue and a small digital part, the standalone flow is the one to use. In this flow, the analogue and the digital parts are designed isolated in each domain. Both finished designs are assembled in a system, where the assembly is performed in the analogue domain. Simulations of the complete assembled system can only be performed after a layout integration. For an AMS design with a big analogue part and small digital part, the Analogue On Top (AOT) flow is used. In the AOT flow the analogue system is the top system. It is developed first and the small digital part is included as a subpart. Small digital blocks are implemented standalone using a subsystem floorplan for I/O placement. Afterwards, the finished digital part is integrated into the analogue design. In the AOT flow, the digital part is simulated using the analogue solver. Therefore, the digital part must be quite small containing a low amount of cells. If the digital part is big and the analogue part is small, the Digital On Top (DOT) flow is applicable. Here, the system is designed in the digital environment and the analogue part is integrated into the digital environment. Full custom analogue design is performed until abstract generation. The entire system simulation is performed by the digital solver using timing information of the analogue subsystem. For a complex system, with multiple analogue and digital sections the Mixed Signal On Top (MSOT) flow is used. Here, the system can be designed, verified and implemented in both the analogue and the digital domain. The analogue tools are used for the analogue layout and the digital tools are used for the digital layout.

Cadence IC

The Cadence IC package includes a wide range of tools for a digital, analogue and mixed-signal design and implementation. For analogue and mixed-signal designers, this package includes tools for: SPICE/fast-SPICE/mixed-signal simulation (SPICE, Verilog-A/AMS, VHDL-AMS), Spice Radio Frequency (RF) analysis, schematic capture, simulation management (including montecarlo analysis), custom characterisation environment, circuit optimisation, yield optimisation, parametric sensitivity analysis, Layout editing, Schematic driven layout (constraint aware), Complex device Module Generator (MODGEN), Full custom floorplanning , Cell/block placer, Layout migration, Cell/chip routing, Interactive Design Rule Check (DRC), Extraction Register Clocks (RCLKs), Layout Versus Schematic (LVS), DRC, Electromigration analysis, IR Drop analysis as well as support for multiple design database formats (CDB and OpenAccess). For digital designers this package includes tools for: logic simulation (covering VHDL, Verilog, SystemC, SystemVerilog, SystemVerilog Assertions (SVA), Property Specification Language (PSL) and e), formal property proof, verification planning and management (and Verification Intellectual Property (IP)),

Synopsys Design Constraint (SDC) checking and exception generation, Clock Domain Crossing (CDC) checking, Register Transfer Language (RTL) (Verilog, SystemVerilog and VHDL) synthesis, high level (C/C++/SystemC) synthesis, test insertion, physical implementation (Placement, Clock Tree Synthesis (CTS), Routing, and Optimisation), logical quivalence checking, RC extraction, DRC, LVS, signoff timing analysis, signoff power analysis, standard cell library characterisation/re- characterisation, and Automatic Target Generation Process (ATPG).[155]

SYNOPSIS

Synopsis offers a wide range of software packages for different applications. For example the Front End and Verification Suite (FEV) for verification and synthesis of digital designs for ASICs and FPGAs targets. The Application-Specific Instruction-set Processors (ASIP) designer, a tool for Application-Specific Instruction-set Processors (ASIP) for applications benefiting from highly specialised processing elements that are programmable in C. The ASIC Implementation Suite (IMP) includes a range of tools for physical implementation of digital designs and physical design signoff. The ASIC IMP includes tools for the Physical implementation (Floorplanning, Placement, CTS, Routing, and Optimisation), RC extraction, DRC, LVS, Signoff Rail analysis. The Analogue Simulation and Modelling (ASM) suite includes a wide range of tools for full-custom design, analogue circuit simulation and verification as well as mechatronic system modelling. The ASM suite includes custom compiler for full custom design plus a range of SPICE and Fast-SPICE, RF simulation capabilities. The Saber tool, included within the ASM suite offers multi-domain modelling (with VHDL-AMS or MAST HDL) covering a wide range of physical systems (electrical, thermal, mechanical, magnetic, hydraulic, etc.), all integrated with schematic capture, simulation and result analysis. The advanced Technology Computer Aided Design (TCAD) suite provides an extensive set of tools for the semiconductor process and device modelling, with an integrated analysis scenario exploration environment. The advanced TCAD suite includes tools for; Two-Dimensional (2D)/3D process simulation and modelling, structure definition, device simulation, compact model generation, and 2D/3D interconnect field solvers. The System Level (SYSL) Suite offers Platform Architect and Virtualiser to develop executable virtual prototypes.[156]

Mentor Graphics

For the digital design, mentor implementation solutions, Oasys-RTL™, Olympus-SoC™, Nitro-SoC™, and Calibre® InRoute™deliver innovative technologies are available for fast and high-quality design closure at advanced process nodes. Mentor graphics also offers mixed-signal solutions such as Analog FastSPICE™, Symphony Mixed-Signal Platform, Questa ADMS™, Solido Variation Designer and Solido ML Characterization suite.

Table 5.1: Manufacturing processes by ams [159]

Process Name	Min Draw Poly	Metal Layers	Operating Voltage	HV Devices
C35B4C3	0.35 µm	3-4	3.3 V and 5 V	-
H35B4D3	0.35 µm	3-4	3.3 V and 5 V	120 V
A30	0.3 µm	3-4	3.3 V	-
aC18A6DMCA	0.18 µm	6	1.8 V and 5 V	-
aH18A6DMCA	0.18 µm	6	1.8 V and 5 V	120 V

The Analog FastSPICE™(AFS) Platform is the world's fastest nanometer circuit verification platform for analogue, RF, mixed-signal, and custom digital circuits. Eldo Platform is the industry proven, most advanced circuit verification platform for analogue-centric circuits. It offers differentiated solutions for reliability verification and comprehensive circuit analysis and diagnostics for analogue, RF and mixed-signal circuits in automotive, industrial, medical and other mission-critical analogue-centric ICs. The Symphony Mixed-Signal platform is the industry's fastest and most configurable mixed-signal solution to accurately verify design functionality, connectivity and performance across A/D interfaces at all levels of the design hierarchy and for all IC applications. Questa ADMS™gives designers a comprehensive environment for verifying complex AMS SOC designs. Analogue and mixed-signal SOC designs combine analogue and digital content more tightly than ever before. They increasingly depend on integrated analogue blocks such as ADC and Digital To Analogue Converter (DAC) converters, phase-locked loops, and adaptive filters.[157]

5.1.2. Design Kits

For design tool driven ASIC design, designs PDKs are provided by foundries. PDKs support full custom design for the schematic driver process, including standard cell libraries, technology files, Parametrized Cells (PCells), design rules file, timing files etc. For the digital layout, PDKs include digital standard cells, including timing information and abstract layout cells. PDKs are offered by On Smiconductor®, ams, IHP Globalfoundries®, TSMC, UMC and X-FAB.

On Smiconductor® offers I3T50, I3T80 and ONC18/I4T supporting up to date development tools [158]. The PDKs from On Smiconductor® support Cadence and Mentor tools and SYNOPSIS for development [158]. AMS designs can be developed using Cadence or Mentor design kits. Synopsys only supports the digital design flow.

PDKs distributed by ams are called High Performance Interface Tool

Kit (hitkit), they offer 0.35 µm, 0.3 µm and 0.18 µm processes as listed in Table 5.1. In 2018 ams announced the End of Life (EoL) of its 0.18 µm processes. The A30 process is a pure analogue process for low noise design. Therefore, the C35 and H35 processes are suitable processes for this project: all of them are only supported by Cadence IC [160]. Advantage of the H35 high-voltage processes is that the C35 process is included in the PDK. In addition to the digital standard cells available in two sizes, analogue standard cells, such as Operational Amplifiers (OP-AMPs) as well as ADC and DAC are included in the C35 hitkit.

IHP offers design kits in 0.25 µm and 0.13 µm technologies. The analogue and mixed-signal flow is supported by Cadence 6 [161], whereby the pure digital design flow is also supported by Mentor Graphics and SYNOPSIS tools. High voltage processes only support up to 20 V. Globalfoundries® offer 0.28 µm, 0.40 µm and 0.55 µm technologies, however, no high voltage technology is available. Supported voltages are up to 3.3 V. They cooperate with Cadence for the design kit creation but also support Mentor Graphics and SYNOPSIS for digital and analogue design flow.

X-FAB offers 0.18 µm and 0.35 µm technologies which can be used in Cadence IC, Mentor Graphics and SYNOPSIS. High voltage technologies allow voltages up to 200 V.

5.1.3. Used Software Tool And Design Kit

Comparing the design tools introduced in Chapter 5.1.1 for a AMS design, Cadence IC and Metro Graphics can be identified as suitable design tools. In contrast to SYNOPSIS, both Cadence IC and Mentor Graphics have a full design flow for a mixed-signal development included. SYNOPSIS is leading for pure digital implementations with a good RTL to Gerber work flow. For custom design and mixed-signal design, Cadence IC is the industry standard and has a better tool set combination with an easy to use mixed-signal simulation tool. Verification tools from Mentor for DRC, LVS and RC-extraction can be integrated in Cadence. Furthermore, all design kits are supported by Cadence IC, therefore allowing a higher flexibility.

Analysing the functionality, size, analogue and digital cells and supported design tools, the ams hitkit is the most suitable design kit for this project. It is planned to create a fully integrated LED driver with the possibility to drive more LEDs in series. To achieve this, a process with high voltage functionality has to be chosen. ams hitkit H35 offers high voltages technology up t 120 V and OP-AMPs and ADC/DAC modules. For Cadence CI ams also offers special tools with Graphical User Interface (GUI) to create start-up scripts. For example, a tool to configure encounter corresponding to the hitkit is available.

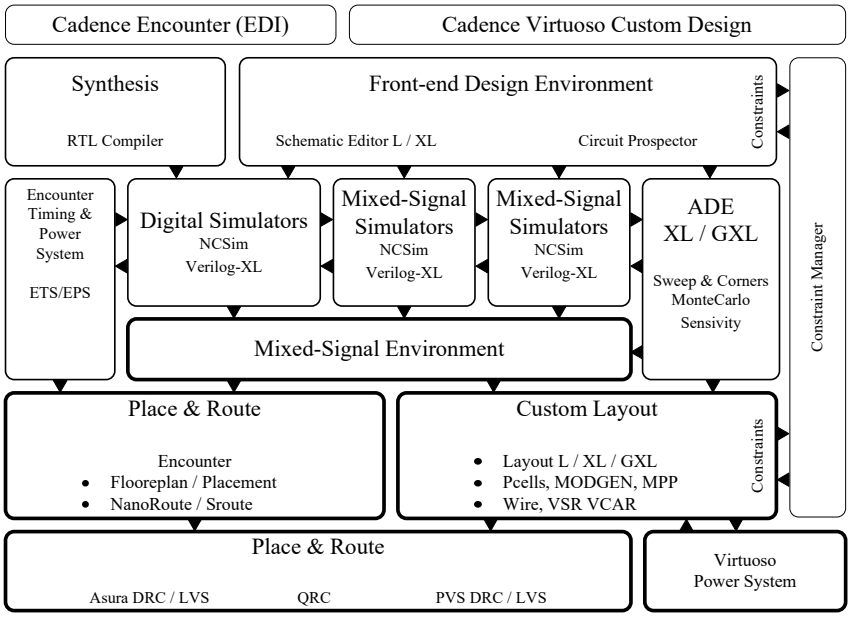


Figure 5.1: Cadence AMS design flow including digital flow on the left using Cadence Encounter (EDI) and the analogue flow on the right using Cadence Virtuoso Custom Design [162]

5.2. AMS Design Flow

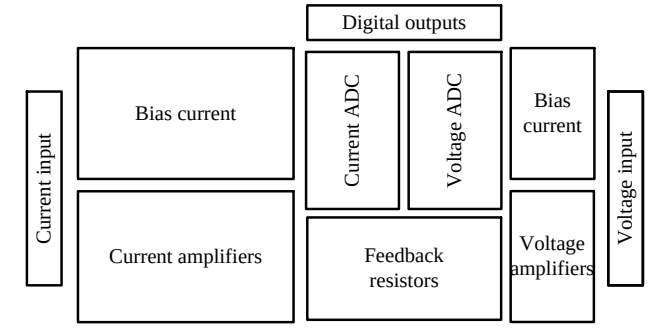
Based on the discrete system, the current controller and the DTM are integrated into an ASIC. This chapter describes the ASIC design starting by an introduction to the AMS design flow followed by the analogue design for current and voltage measurements of the LED. After implementing the analogue part, the digital part is generated out of the developed VHDL code. Furthermore, an outlook to the implementation possibilities for converters is given. Three possible design flows for AMS systems have been introduced in Chapter 5.1.1. In this project the size of the digital and the analogue part of the system is nearly the same. Except the MSOT, both AOT and DOT design flows are applicable. Hence, the AOT design flow has better and easier to use analogue simulation tools, it was used for this design. The overall design flow of the Cadence IC tool is shown in Figure 5.1. It is divided into two sub-flows, analogue and digital, where each flow has an individual tool kit. Cadence Encounter is a special tool set for the digital development which is used to generate the digital sub-design. Part of Encounter is the synthesis with RTL compiler and the Timing and Power system toolbox. Timing models and synthesised designs are simu-

lated in the digital simulation environment using NCSim. The simulation tool uses the gates from the design kit for the simulation including the internal signal timing information. For analogue design Cadence Virtuoso is available which includes a schematic editor and simulation tool set. The Cadence Virtuoso tool set is specialised on the full custom analogue design. The synthesised, placed and routed digital part can be included into the design flow. Designed schematics can be simulated using ADE including sweep, corners and MonteCarlo simulations. ADE allows to use the mixed-signal simulation environment. Thus, ADE is used with a mixed-signal simulation configuration for the entire system verification. So far, the simulation tools have no placement and routing informations for the simulation. Both the digital and the analogue designs are placed and routed individually. From the placed and routed digital and analogue part, the RC-extraction is performed to identify a full analogue system for simulation including parasitic resistors and capacitors in the system. A full system simulation is performed using the placed digital part combined with the analogue part. In addition, the RC extraction information is simulated for all placed transistors using the analogue solver which is time-consuming.

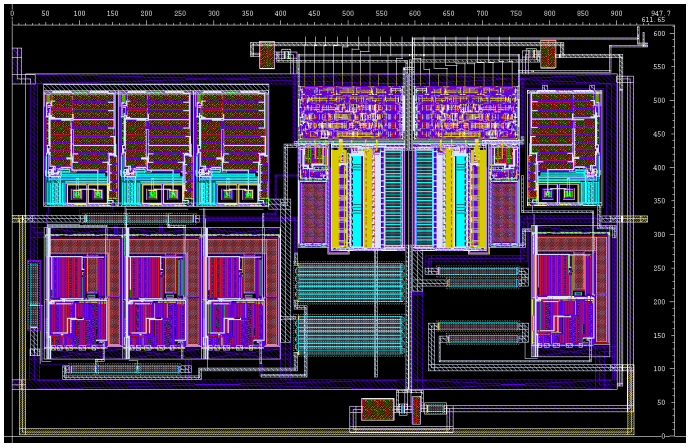
5.3. Analogue Design

The analogue implementation process starts with the definition of specifications and the choice of a technology. After defining the specifications and the technology, the analogue design needs to be implemented. The implementation is performed by a schematic driven implementation with a previous schematic simulation. For the schematic simulation a test bench has to be developed defining the external signals needed for the simulation. First, the functionality of the schematic is simulated and the results are analysed. When the functionality of the schematic is confirmed, more advanced simulations are performed including corner analysis and MonteCarlo analysis and optimisations. Using the schematic driven implementation approach, the elements or devices used in the schematic are generated in the layout automatically. The connection must be routed manually. When the layout is finished, a DRC and LVS are performed to check if the design rules are followed and no deviations to the schematic exists. Extracting the parasitic from the resulting layout, a post layout simulation can be performed to check signal propagation times.

The analogue part of the system consists of the current and voltage measurement and the ADCs. For current and voltage measurements, predefined OP-AMPs from ams are used. In hitkit C35 and H35 three operational amplifiers are available; OP05B, OP_LN and OP_WB. Each is designed for a special application. OP05B is an internally compensated OP-AMP with P-Type Metal-Oxide-Semiconductor (PMOS) input stage and is de-



(a)



(b)

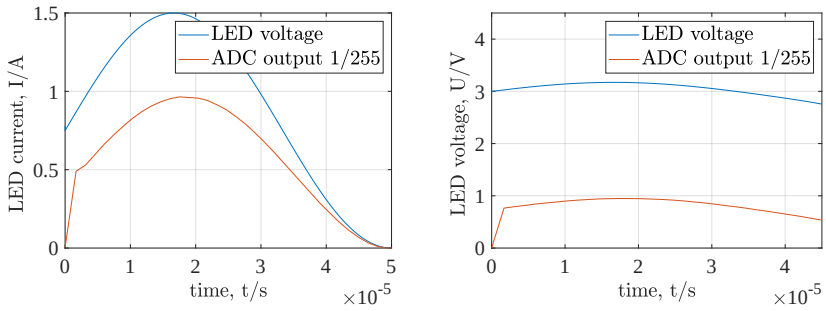
Figure 5.2: The floorplan of the analogue part of the ASIC (a) and the analogue part of the chip including voltage and current measurements with size information (b)

signed for low power switched capacitor applications [163]. OP_LN is an internally compensated OP-AMP for low noise applications with a provided power down mode [164]. OP_WB is a internally compensated OP-AMP for high capacitive loads [165].

5.3.1. Current And Voltage Measurement

The internal current measurement is again performed by using an external shunt resistor. Measuring the current internally will increase the size of the ASIC substantially. Because of the high forward current of the LED of up to 1.5 A, a huge amount of input and output as well as a big internal resistor or current mirror pads have to be used. By using a small external

shunt with a resistance of 0.02 Ω, like in the discrete design for the current measurement, an internal amplification of ≈100 is needed. The best fitting OP-AMP for this purpose is the OP_WB, because it can drive the input stage of the ADC, a sample and hold stage with an input capacitance of 3 pF [166]. Since the OP_WB is not a rail to tail OP-AMP, the voltage across the shunt has to amplified using a differential amplifier with a reference voltage. This reference voltage is set to 1 V using a voltage divider followed by a voltage follower. To achieve a high amplification, two differential amplifiers are used in series. Together they have an amplification of 90, resulting in an output voltage rage of 0.07 V to 2.7 V for an input current range of 0 A to 1.5 A. This is similar to the values of the used INA in the discrete implementation with an amplification of 100. The output of the amplifier is connected to the 8 bit ADC, a part of the analogue library from ams. ams ADC8 is a Successive Approximation Register (SAR) ADC with a maximum conversion frequency of 10 kHz which is sufficient for this design (cf. Chapter 4). To achieve maximum resolution of the ADC, the reference voltage pins are connected to the amplifier output voltage 0.1 V to 2.8 V. Each reference voltage is generated using a voltage divider consisting of an FET and a poly resistor. The lower voltage of 0.1 V is created by using a p-channel FET and the upper voltage of 2.8 V is created by using a n-channel FET. In contrast to the current measurement, the voltage measurement does not measure a voltage in reference to ground (cf. Figure 4.1). The voltage across the LED is the difference between the top and the bottom LED pin. Here, a difference amplifier using one single OP-AMP is applied. The amplification of the difference amplifier is set to 0.87 to enable the measurement of the maximum forward voltage of the LED of 3.25 V by an internal supply voltage of 3.3 V. For the current measurement the output of the voltage amplifier is connected to an 8 bit ADC. The output voltage of the voltage amplifier can rage from 2 V to 2.8 V. Therefore, the reference voltages for the ADC are configured to 2 V and 2.8 V. Because both voltages are relative high, the reference voltages are created using n-channel FETs and a poly resistor. The combination of current and voltage measurement completes the analogue design. Each OP-AMP needs a bias current generator included in the ams hitkit H35. The overall analogue design consists of four OP-AMPs, four bias current generators, two ADCs and several resistors and transistors. By placing the ams standard cells, the design size is defined to 880 µm x 470 µm. For an easy connection of the digital and analogue part, the ADC outputs are placed in series on the top side of the design. Inputs for current and voltage measurement are placed at the side directly next to the OP-AMPs input. The full analogue schematic is shown in Appendix C. Inputs of the analogue design are the analogue supply voltage of 3.3 V, ground, clock for the ADCs, positive LED voltage and negative LED voltage. Outputs are end of conversion and 8 bit of both ADCs. Figure 5.2a shows the floorplan for the analogue part of the



(a) (b)

Figure 5.3: Simulation results from Cadence IC showing the transmission rate of both amplifiers and ADC for (a) current and (b) voltage across the LED

ASIC, the resulting analogue design is shown in Figure 5.2b.

5.4. Digital Design

To conclude the design, the digital part also needs to be synthesised and placed. In contrast to the analogue design flow, the digital design flow uses a design description in RTL coding. The design description is taken from the discrete design introduced in Section 4.2. For the implementation of the VHDL code, the code has to be adopted to fit into an ASIC design. Thus, the intercepts and slopes defined for the discrete design have to be adopted to fit the digital voltages. Furthermore, the digital currents have changed too. This changes the current set points for the current controller. Figure 5.3 shows the simulation results from the amplifier and the ADC. The LED is supplied by a sin wave current from 0 A to 1.5 A and the ADC output is mapped to the input voltage and current. The ADC resolution for current and voltage measurement has changed due to using other internal amplifiers. These values have to be adopted in the temperature determination part of the code. Constants and initialised vectors have to be hard-wired with reference blocks for logical low and logical high which are available in the digital part of the ams hitkit. With a fitting test-bench the changed code is simulated to check its basic functionality. In contrast to the FPGA synthesis, the ASIC synthesis creates standard cells, i.e. OR, AND, NAND, resulting in a netlist of gates. After the synthesis, information about propagation delay can be included into the simulation. When the simulations with propagation delay result in full functionality, the standard cells in the netlist have to be placed and routed to generate a finished layout.

5.4.1. VHDL Implementation

Part of the place and route process is an optimisation and a clock routing. For the ASIC synthesis, the three variations of the forward voltage method introduced in Chapter 2.4.1 are synthesised, placed an routed again. After simulating, the design can be placed using the Cadence Encounter RTL compiler. In Encounter the size, boundary conditions and I/O ports have to be defined. The analogue part of the chip has a size of 950 µm x 610 µm, as shown in Figure 5.2. The overall chip design should have a square or rectangular shape, therefore the 950 µm side of the analogue design is used for width condition for the digital placement. Choosing the same side length of the analogue and digital part inhibits waste of space. The connection port of the analogue measurements to the digital part is placed on top of the analogue design, which can be seen in Figure 5.2. To allow short connections with stubs between both parts, the connection pins are placed in the same order and distance on the bottom side of the digital part. Because the side length of the digital part is fixed, the height of the digital part can be adapted only. The height is determined by the space needed by the placed and routed system. For the biggest, the quadratic approach, a minimum size of 405 μm^2 is required to perform placement and routing. To enable a lower density of the system and a degree of freedom for optimisation, the height is predefined to 533 µm. All outputs are placed on the top side of the digital design. This allows a short connection to the I/O pads of the finished chip. After adding the supply rings around the edge region of the digital part, an area of 880.6 µm × 488.8 µm can be used for placement. The cell density gives information about the overall space used in the different designs. After defining the floorplan, the standard cells are placed including a pre-place optimisation. The placement is optimised using the clock tree synthesis optimizer. Afterwards, the clock tree is synthesised followed by the post clock tree synthesis optimisation. The final step is routing of the signals between the standard cells. Filler cells are used to fill the free space between the standard cells and the supply lines. This is performed for all approaches to get information of the resulting size. Figure 5.4 shows the resulting design of the quadratic approach. Table 5.2 indicates the number of placed cells, the density of the digital part and the area used for each approach. Placement, optimisation and routing needs a degree of freedom to achieve highly optimized results. Therefore, a density above 90 % is not applicable. As expected, the pulsed approach needs the least amount of space and number of cells. Using this approach, the design can be reduced in size. The linear approach requires 1.7 times the space of the pulsed one. The quadratic solution needs most space and number of cells which is more than double the resources of the pulsed approach (cf. Table 4.2). The timing analysis shows that each design can be clocked at 200 MHz which is the same clock frequency used on the FPGA test board.

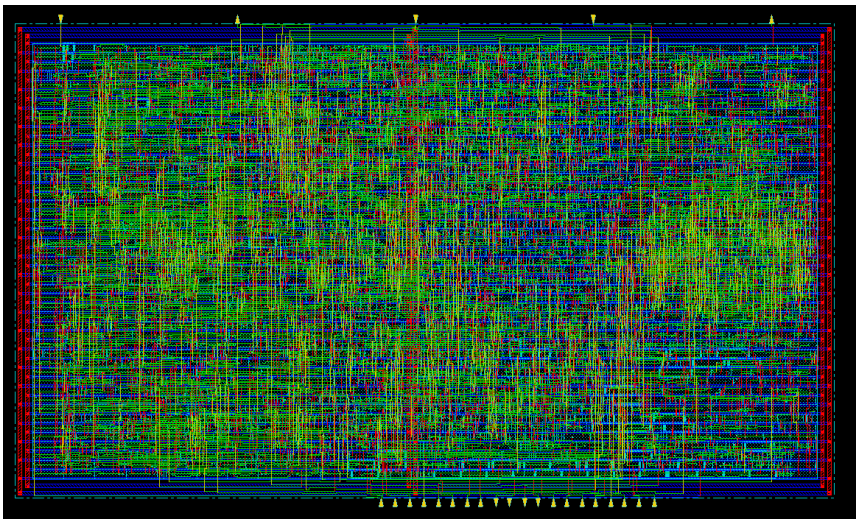


Figure 5.4: Placed and routed design of the linear approach with 67.95 % density. Pins for communication are on top, pins to the analogue internal part are on the bottom edge

Table 5.2: Cadence Encounter RTL compiler placement report showing the density of the 950 µm x 533 µm digital part

	linear	quadratic	pulsed
Cells placed	3389	4368	1802
Density	76.95 %	95.02 %	42.3 %
Used area	327 527 µm^2	404 404 µm^2	179 976 µm^2
Fabrication cost	210 €	260 €	115 €

5.5. Layout

To finish the ASIC, the analogue and digital part have to be connected. Analogue outputs and digital inputs are placed directly next to each other whereby the connections can be performed using parallel lines. Inputs and outputs of the ASIC have to be connected to I/O pads and the supply voltages have to be connected to supply pads. All pads are placed in an I/O ring around the active chip region. Before placing the pads in the ring, the chip package has to be identified to check whether the bonding rules are followed. The angle between the edge of the die and the bond-wire has to be at least 45° [167]. The ASIC has 15 I/Os, therefore a good fitting package for the design is the QFN16 (5 x 5) package with 16 pins, with 4 pins on each edge. To follow the 45° rule for the bonding dia-

gram, maximum four pads can be placed on each side of the the I/O ring. The digital as well as the analogue part are supplied by 3.3 V. To reduce feedback effects from digital to analogue and backwards, the I/O ring is split into two parts, an analogue and a digital part using power cut cells. ams hitkit offers a variation of I/O and supply pads. Supply pads are available in 3.3 V and 5 V technology connecting the supply ring lines with the corresponding supply level. Analogue and digital I/Os have an integrated Electrostatic Discharge (ESD) protection and can be found for a high variation of applications. Analogue I/O pads are available with different series resistances of 0 Ω, 50 Ω, 100 Ω, 150 Ω, 200 Ω and 1500 Ω. For this design analogue I/O pads with 200 Ω are used to achieve sufficient safety without charging the drivers too much. Digital I/O pads with pull-ups and pull-downs as well as fast and slow drivers are available. Furthermore, the driving strength can be chosen from 2, 4, 8 and 16. Open drain output with pull-up and pull-down and Schmitt Trigger output are available too. Additionally, special input pads for clock signals and configurable pads which can be switched from input to output by the ASIC pads, can be used. For the reset input a digital input with pull-up is used, for the clock input the special clock pad is used with a driving strength of 4. The two digital outputs are connected by standard output drivers with a driving strength of 4. After placing the I/O cells and the power cut cells in the ring, the ring is filled up with filler cells. The I/O pads need a supply for the driver, pullup and pulldown. Therefore, they are connected to the supply pads using filler cells. Including the I/O ring of the chip, the overall chip size is 1884.4 µm x 1884.4 µm. Figure 5.5a shows the complete ASIC with I/O-ring and Figure 5.5b shows the bonding diagram for the QFN16 package. The pin description can be found in Table 5.3.

5.6. Summary

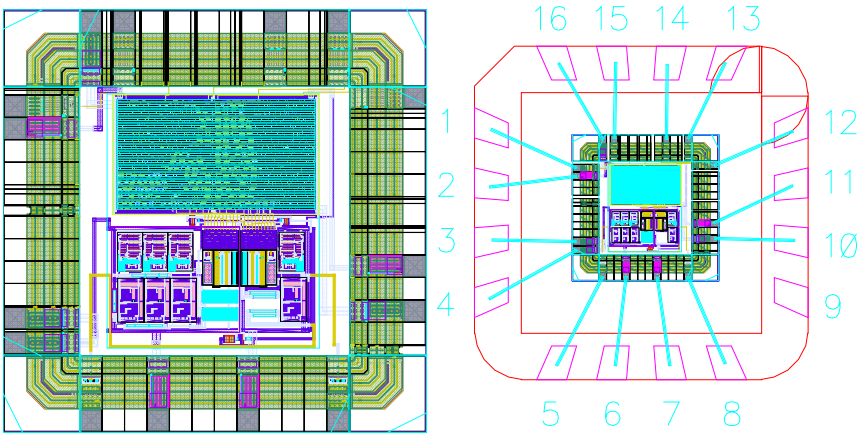
In this chapter the ASIC design for the LED driver with internal thermal management is shown. First, design methodologies for LED driver integration are shown including a list of available ASIC development tools. Especially of digital CMOS design, design kits are available on the market including digital standard cells needed to synthesis the RTL design into the ASIC. Some of the design kits also include analogue standard cells, i.e. OP-AMP, ADC and DAC. The most common design kits and included standard cells are listed in this chapter. It is planned to create a full integrated LED driver ASIC for more than one LED, therefore the supported voltage levels are important. On Smiconductor® and ams offer design kits with high voltage technologies which are applicable for this project. In contrast to On Smiconductor®, ams includes more analogue standard cells which can be used for the voltage and current measurement. ams offers design kits (hitkits) for 350 nm for standard applications (C35) and high voltage (H35).

Table 5.3: Pin number and functionality of the ASIC

Pin Number	I/O	Name	Description
1	Input	Clock	100 MHz to 200 MHz system clock
2	Supply	DGND	Digital ground
3	Supply	AVDD	Analogue supply
4	Supply	AVDD	Analogue supply
5	I	V_{LED} -	Negative LED voltage input
6	Supply	AGND	Analogue ground
7	Supply	AGND	Analogue ground
8	I	V_{LED} +	Positive LED voltage input
9	-	NC	Not connected
10	Supply	Digital VDD	Digital supply
11	Supply	Digital GND	Digital supply
12	O	UART TX	UART transmit
13	I	UART RX	UART receive
14	I	RESET	Chip reset
15	O	PWM	PWM out for step-down converter
16	Supply	Digital VDD	Digital supply

Both are only supported by Cadence IC software tools, thus Cadence IC tools are used for this design. After identifying the design tool and the design kit used for this design, the AMS flow of Cadence IC was shown. The flow is divided into digital design using Cadence Encounter and analogue using Cadence Virtuoso. The results from the previous Chapter 4 were used as basis for the overall ASIC design. The analogue design is based on the discrete design on the external extension board of the ATLY development board and the digital design is synthesised from the VHDL code used to configure the FPGA.

For current and voltage measurements, pre-amplifiers were designed using the included OP-AMPs in the ams hitkit. The current measurement was performed with an external shunt of 0.02 Ω. To digitise and measure the voltage across the shunt, it has to be amplified by 90, similar to the discrete design. Two differential amplifiers are built with the OP_WB form the hitkit which output can drive the sample and hold of the ADC. For the forward voltage measurement, a differential amplifier with an amplification of 0.87 is used, to reduce the maximum forward voltage of 3.25 V to a voltage in the operation region of the OP-AMP and the ADC. Both ADCs have reference voltage inputs. Four internally needed reference voltages



(a) (b)

Figure 5.5: Layout of the complete ASIC, digital connected to analogue and with I/O ring and (a) bonding diagram of the ASIC for a QFN16 (5x5) package(b)

are generated because different reference voltages are used for the current and the voltage measurement. By connecting the amplifiers with the ADCs the analogue design was completed. The outputs of the ADCs of the analogue design are placed along the upper edge of the layout. This allows to place the digital part at this edge using short wires for the connection. Using this floorplan, the side length of the digital design was predefined. To get information about the area required for the digital placement and routing, the VHDL code was synthesised. The VHDL code had to be adopted to get synthesiseable using the ams hitkit. Constant values are connected to hard-wired reference blocks for logical low and logical high. After synthesising the quadratic approach, the height of the design was defined to 533 µm to consider a degree of freedom for the optimisation logarithm of the placement. In the layout, the connections to the digital part are placed in the same order as those in the analogue part. External I/Os are placed on the top edge of the design. One supply ring is created around the digital area with one additional central supply bar to supply all digital gates. Similar to the FPGA implementation the quadratic approach requires most space and number of standard cells, followed by the linear approach and the pulsed approach. For the ASIC design, the linear approach was implemented which is the best fit in terms of required space and accuracy. At the given size of 533 µm, the linear approach results in a density of 76.95 % which is low enough for the optimisation process to work properly. After connecting the analogue and the digital part, an I/O ring was created around the design resulting in an overall size of the ASIC

of 1884.4 µm x 1884.4 µm. Hence, the design has 15 I/Os in total, it was packed into the best fit package, the QFN16 with 16 I/O pins.

6

ASIC Implementation To an LED System

For a moment, nothing happened.
Then, after a second or so, nothing continued to happen.

Douglas Adams

To test the finished and produced ASIC, a test PCB is developed containing all necessary peripherals for the design. Corresponding to Chapter 3.2 and Chapter 4.1 an equal step-down converter is used with an inductance of 6.8 µH and a capacitance of 100 µF. The same shot key diode for free run is used on the test PCB. The used structure of the step-down uses a high side switch. Therefore, the PWM output of the ASIC has to be shifted to the supply level to ensure a closed MOSFET with a high $R_{DS(on)}$. This task is performed by an comparator from Texas Instruments Inc., the LMV7219. The reference voltage for the comparator is created by a voltage divider with a factor of $\frac{1}{3}$ resulting in a reference voltage of 1.6 V at a supply voltage of 5 V. Thus, simulation results from Chapter 5.4.1 show that the ASIC can be clocked by 200 MHz. A crystal clock oscillator with a frequency of 200 MHz is placed on the test PCB. For testing purpose, the clock can be changed to a 100 MHz clock. The 3.3 V supply voltage for the digital and analogue part of the ASIC is generated using the TPS62111 from Texas Instruments Inc. providing a stabilised supply voltage. Each supply pin of the ASIC is buffered by a 100 nF capacitor. The test design is completed by a FTDI chip translating the UART signals to Universal Serial Bus (USB) communication. Figure 6.1 shows the test PCB with mounted ASIC including step-down converter, LED, power supply and communication interface. For the discrete design, the conversion of the current to the 8 bit values for the current set point is calculated using (4.1). The current amplification in the ASIC is slightly different to the INA214 used in

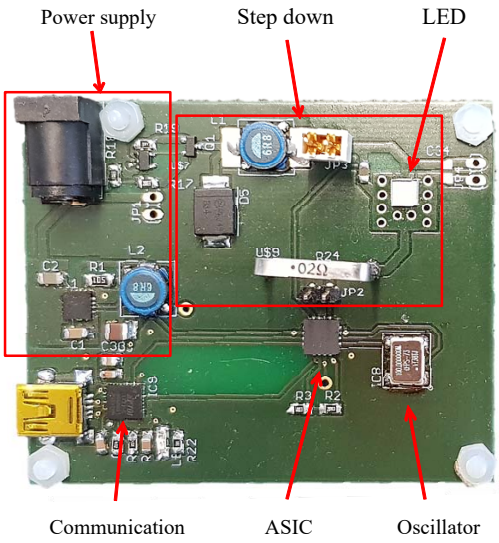


Figure 6.1: ASIC soldered on the test PCB including step-down converter LED, power supply and communication interface

the discrete design. Furthermore, the reference voltages of the ADC differ. Thus, the 8 bit values have to be recalculated using information about the new hardware structure. This results in a calculation for the ASIC current controller (6.2).

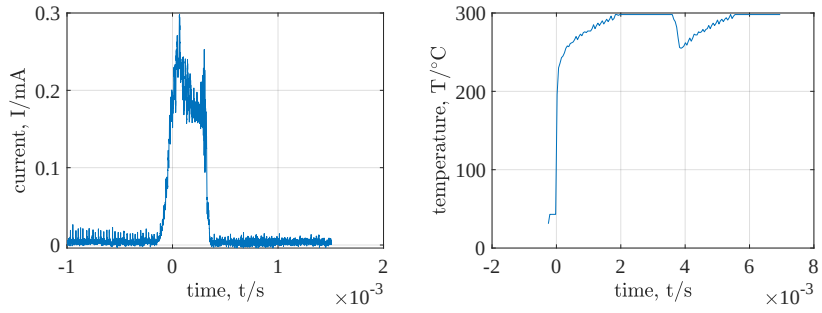
$$I_{ADC} = V_{0.02} \cdot P_{iamp} \cdot m_{ADC} - b_{ADC} \tag{6.1}$$

$$I_{ADC} = V_{0.02} \cdot 90 \cdot 94.4 - 9.44 \tag{6.2}$$

P_{iamp} is defined in Section 5.3.1 as 90, m_{ADC} =94.4 and b_{ADC} =9.44 are identified from the mixed signal simulation in Cadence IC (cf. Figure 5.3). In the ASIC an initial start current value of 254 is defined which represents 1.5 A. The board layout as well as the schematic of the test PCB are shown in Appendix C in Figure C.1 and Figure C.2 respectively.

6.1. Experimental Results

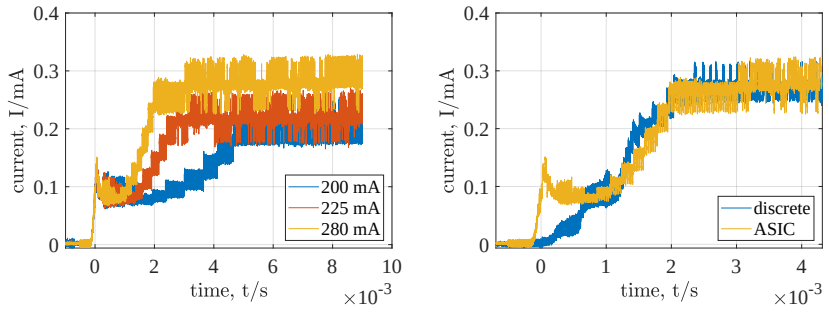
When the test PCB is supplied with 5 V, the LED is driven with the initial constant current of 1.5 A provided by the current controller. This current can be adjusted by sending an 8 bit value to the ASIC in the same way as for the discrete design in Section 4.1. The amplification of the internal current amplifier of the ASIC is configured using poly resistors. These poly resistors have a tolerance and cannot be produced with exact resistor values.



(a) (b)

Figure 6.2: Measured current controlled by the ASIC after boot (a) and determined temperature of the LED using the forward voltage method (b)

This results in a different LED current compared to the values calculated by (6.1). At the beginning, the internal temperature controller design in Section 4.3 is active, too. The temperature determination uses the internal forward voltage measurement. Similar to the current measurement, poly resistors are used to set the gain of the OP-AMP amplifier. Because of structural differences in the thickness of the poly layer these resistances and thus the gain differ. The identified temperature does not fit the exact temperature of the LED. Compared to the real temperature of the LED, the internally measured temperature of the ASIC is much higher. With a current of 200 mA at room temperature (20 °C), an LED temperature of up to 300 °C is detected as shown in Figure 6.2b. The identified temperature of maximum 300 °C leads to an active thermal management and the current is reduced to nearly 0 A as shown in Figure 6.2a. To overcome this fact, the predefined internal slope and intercept values for the temperature determination have to be changed. To modify theses values, the same protocol as in the discrete design is implemented in the ASIC. By transmitting a 255 via the UART interface the ASIC switches into configuration mode. Afterwards the new slope and intercept values can be transmitted. Each slope and intercept value is an 11 bit vector. An UART interface allows to transmit 8 bit, this is why the slope and intercept values have to be divided and transmitted in two transmissions. The first transmission contains the lower 8 bit of each value and the second transmission the missing upper 3 bit. After the two transmissions are received by the ASIC, the corresponding intercept or slope value is changed. To change all nine slope and intercept values, all in all 19 transmissions are necessary, including the start transmission. When the ASIC has received the 19 transmissions, it expects a current set point again. A problem which arises for the adjustment of the values is that the internal measured voltages and currents are



(a) (b)

Figure 6.3: LED current with a set point of 400 mA, 450 mA and 550 mA using the ASIC as a pure current controller with deactivated DTM (a) and the comparison of the step response of the ASIC and the one from the discrete design with same height

unknown and are not transmitted through the UART interface. This fact makes the determination of the correct values for the internal current and voltage measurement of the ASIC impossible. To check the functionality of the current controller, all slope and intercept values are configured to 0. This leads to a continuously measured temperature of 0 °C which changes the mode of the ASIC to a standard LED driver without thermal management. After performing these changes, the current controller works similar to the discrete controller and the settle times are similar to the test results performed for the discrete system listed in Table 4.1. Figure 6.3a shows the step responses for three currents. These are the only possible currents of the system because of the error in the internal amplification of the current measurement. Values transmitted to the ASIC smaller than 250 will result in a low forward current below 100 mA. By transmitting the value 250 to the LED driver the current is set to approximately 200 mA (blue line in Figure6.3a). Transmitting a 251 result in a current of ≈225 mA and a 254 to 280 mA. At these low currents the PWM steps of the output current can be easily identified. Nevertheless, rise times of 2 ms to 4 ms are achieved which is comparable to the discrete driver design. Figure 6.3b shows the highest possible step response of the ASIC compared to a step response with a similar current from the discreet design. With the exception of the steep pike at the beginning, the two step responses are very similar. Settle times of both controllers is approximately 2 ms. These results show that the current controller works similarly to the one of the discrete system but the current measurement has to be adopted to enable higher forward currents of the system. In the current version a two stage amplifier is used to realise the high amplification of 90. A better amplification setup can be achieved by using rail to rail OP-AMPs to create an instrumentation ampli-

fier. Same is possible for the voltage measurement.

6.2. Summary

In this chapter a test PCB is developed to test the produced ASIC. Parts of the PCB are power supply, communication interface, ASIC clock and the step-down converter including the LED and the shunt for the current measurement. The internal amplification for the current measurement of the ASIC differs slightly from the used amplification in the discrete design. Therefore, the values for the current set points used for the discrete design have to be adopted. The step response is tested using the current controller. At power on state the LED should be supplied by 1.5 A, the LED only lights up a bit with a current of 200 mA. Parallel, the ASIC transmits the internal determined temperature via the UART interface. It is detected that the internal determined temperature of the LED is approximately 300 °C. The reason for the misinterpreted temperature seems to be related to high variations of the internal feedback resistors of the OP-AMP amplifiers. This variations result in variations of the amplification and misinterpreted voltage and current. For the temperature determination the measured voltage and current are used, with the variation in both, current and voltage the temperature is not determined correctly. This misinterpreted temperature is the reason for the low output current, the internal DTM reduces the drive current of 1.5 A to 200 mA to cool down the LED. By a specific transmission protocol, the DTM behaviour can be changed or deactivated. To adopt the temperature determination of the DTM, the slopes and intercepts have to be changed to fit the real temperature. The internal measurements of current and voltage are not transmitted and are therefore unknown. Thus, it is impossible to adapt the DTM values to enable a correct temperature determination. The DTM is deactivated to test the current controller of the ASIC without using the DTM. After deactivating the DTM, it is recognised, that the internal current measurement varies more than expected. The current controller can only be used in a small rage of 200 mA to 280 mA. A possible reason for this could be the two stage amplifier design for the current measurement. However, the current controller step response timings are comparable to the discrete design. By a further development of the current and voltage measurement system the ASIC will work in the same way as the discrete design.

7

Conclusion

And to this end they built themselves a stupendous super-computer which was so amazingly intelligent that even before its data banks had been connected up it had started from I think therefore I am and got as far as deducing the existence of rice pudding and income tax before anyone managed to turn it off.

Douglas Adam

Current white light LEDs for lighting purposes are increasing in efficiency over the last decades. Nevertheless, they still do not provide 100 % efficiency and convert power into heat. By this so called self heating, the semiconductor of the LED as well as the colour conversion layer can get damaged or destroyed. The conversion layer is needed since the most efficient LED is the blue LED. To create white light using a blue LED, a colour conversion layer on top of the LED is needed. This layer converts a part of the blue light into yellow light. The mixture of blue and yellow light appears to be white. Thermal effects for both the active region and colour conversion material are listed in Chapter 1. The overheating of the active region of the LED will reduce the lifetime up to 20 %, whereby high temperatures of the conversion layer can shift the colour of the LED and increase the lumen loss in the layer of up to 30 %.

To overcome this internal heating an LED driver with included DTM is needed. Mandatory for a DTM is the knowledge about the internal temperature distribution in the LED. Chapter 2 introduced the structure of white LEDs including the temperature determination methods as well as their accuracy and applicability. Three temperature determination methods were identified as integrability: the linear forward voltage method, the quadratic forward voltage method and the PJTM. The linear forward voltage method has a good accuracy in the operation range of the LED,

the quadratic forward voltage method and the PJTM have a good accuracy even beyond the operation range. For all of them the used LED needs to be calibrated to determine the coefficients needed. For this purpose, a calibration PCB was developed providing current pulses of 0.1 A to 1 A for a short period of <20 µs. This allows to perform measurements at the LED with neglecting the self heating.

Furthermore, multiphysic simulations of LED structures including package and dome were performed. The results show the correlation between the temperature of the active region and the temperature of colour conversion layer. The simulations were performed for a simple LED setup first to test the simulation reliability. Afterwards, simulations of an used LED from CREE® were performed. Structural information was identified by an electron microscope image of the cross section of the used LED. Temperatures of the simulation results were compared to experimental temperature measurements acquired using an infrared camera to validate the simulations. Temperature differences between the active region and colour conversion material were listed in a table. This table was used to prove that the previous identified temperature determination methods can also be used to determine the colour conversion layer temperature.

Followed by the temperature determination, cooling mechanisms applicable for LEDs are introduced. Cooling mechanisms are divided into passive and active. Beside classical cooling methods using a heatsink (passive) or a heatsink with fan (active), new low noise technologies are introduced. Ionic winds and synthetic jets are up to date technologies to cool electric devices. Experimental test setups were developed and the possible air speed and efficiencies were determined. Both technologies were tested as cooling devices for an LED. The thermal resistance from the LED cooling plate to the environment was calculated for both cooling mechanisms resulting in a better performance of the synthetic jets.

Chapter 2 is concluded by listing possible DTM systems for semiconductors and developing an applicable DTM for an LED system. The developed DTM has three states: S_1 where the LED is operated at its desired current with a temperature range of 20 °C to 85 °C. When 85 °C are exceeded, S_2 is activated where the current of the LED is reduced proportionally to the temperature by a ramp function until the LED reaches the maximum operation temperature when the DTM changes. In state S_3, the LED is turned off completely to avoid damages by the high temperature. To measure the current temperature of the LED, a current flow is necessary. In state S_3 the LED is deactivated and no temperature determination is possible. To overcome this, three exit strategies were developed. The first uses a pulsed current mode where the LED is supplied with a low current for a short time periodically to determine the temperature. The second supplies the LED with the lowest possible current of ≈100 mA and the third is an external reset to reactivate the LED driver. When the temperature of

the LED falls below the threshold, the DTM changes back in state S_2.

LEDs have to be supplied with a constant current because of their steep characteristic curve. Chapter 3 introduces LED driver topologies beginning with linear and step drivers, followed by new approaches which combine both. Combining a step driver with a linear driver enhances the efficiency when driving more than one LED string. The step driver provides the voltage drop needed by the LED string with the biggest resistance and a linear driver in each string which controls the current through the LED. Nearly all step drivers need an inductor to smooth the current and to store the energy while the supply is disconnected. Inductors cannot be integrated into an ASIC. Therefore, new driver topologies without using inductors are described to enable a full integrated LED driver. One approach is to use capacitive networks connected in a matrix, the so called charge pumps. Capacitors are charged parallel to the supply level and discharged in series to create double of the supply voltage. The same is possible the other way around to reduce the supply voltage. Another approach uses switches to shorten a part of an LED string and use a rectified sine supply voltage. In the rising quaterwave, the switches are turned off successively until the pike voltage is reached. Afterwards, the switches are activated to supply less LEDs. In this work only one LED is used to evaluate the temperature determination and the DTM. An easy to build and reliable LED driver for one LED is the step-down converter, this is why it is used in this work to supply the LED. At the end of Chapter 3 the design of the step-down converter for a specific LED is described. Part of the design is the dimensioning of passive parts including inductor and capacitor. To provide constant current to the LED, the system including LED switch and diode was identified and a current controller was designed.

In Chapter 4, a discrete test system is shown. The system is based on an Atlys™Spartan-6 FPGA board from Digilent®, a Xilinx® Spartan®-6 LX45 FPGA development board including all peripherals needed for an FPGA. An FPGA board is used because the software developed for an FPGA can be used later to synthesise the digital part of the ASIC as part of the LED driver. The digital part including the current controller, temperature determination and the DTM was developed to be placed in the FPGA. The analogue part consisting of step-down converter, LED, voltage and current measurement with ADC and pre-amplifier is placed on a self developed extension board. By using the VHDCI plug which is available on the development board, the extension board and the development board are connected. After implementing and adapting the designed current controller to the ADCs and pre-amplifiers, the current controller was tested with good results of a settle time of ≈0.8 ms. With a working current controller, the temperature determination was tested. All three variations of the temperature determination were tested using the discrete system. To reduce the calculation effort of the FPGA, the slope and intercept values needed by

each method were redefined taking the restitution of the ADCs into account. The 8 bit output of the ADCs can be directly used to calculate the current internal temperature of the LED. The quadric approach was identified as the method with best accuracy but needing the most resources in the FPGA with 446 registers and 598 LUTs. In contrast, the linear approach has a reasonable error of ± 3 °C in the operation range at each current. When the LED has a temperature of 20 °C at 1 A forward current, the accuracy of the linear approach is approximately at -20 °C. The linear approach needs 346 registers and 416 LUTs, compared to the quadratic approach that are 33 % less resources. Furthermore, the linear approach has an equal accuracy in normal operation mode. For the pulsed approach, the PJTM, the accuracy was determined to -5 °C to -3 °C. The current is reduced for the temperature measurements in this approach what leads to the fact that the temperature is also reduced in this phase. To overcome this temperature reduction and correct the value, a correction value has to be implemented for each forward current. Furthermore, the temperature of the LED cannot be detected continuously. Fast temperature changes could not be detected and the LED can get damaged. For best results, an optimum has to be determined measuring the temperature most frequently without reducing the light output, too. Nevertheless, the PJTM needs least recourse of the FPGA with 219 registers and 165 LUTs. Combining all these results, the linear approach was identified as the best fit approach for this work. Compared to the quadratic approach with similar accuracy in the standard operation range it needs less resources. Compared to the PJTM it is easier to implement and has less disadvantages. Chapter 4 is concluded by integrating and testing the developed DTM from Chapter 2. State S1 from the thermal management is the state where the LED is operated in standard operation mode, nothing needs to be changed for this state. If the temperature exceeds the standard operation temperature, the forward current should be reduced linear with the temperature in state S2. To reduce the implementation effort and the size of the design, the state S2 was adopted from a linear reduction to a stepped reduction. The new stepped reduction has 16 steps and each step is $\frac{1}{16}$ of the desired current. The advantage of a stepped current reduction is the low space requirement in the FPGA and later in the ASIC. The necessary divider needed for the linear reduction is replaced by a bitshifter, adder and subtracter. The temperature region for each step is predefined for the used LED. The used internal DTM results in an LED which cannot overheat by self-heating. When the LED is not cooled sufficiently, the forward current is reduced until the temperature does not rise anymore, thus DTM stays in state S2. In a test, a fan was used to cool down the LED, subsequently the current rises again. If the cooling is sufficient for the LED, the DTM switches back to state S1 operating the LED with the desired current. By selfheating the LED cannot heat up so that the DTM will change in state S3. This is only possible when the LED

is heated externally. To test the state S3 and the exit strategy, the LED is heated using a hot air fan. Results confirm the correct working DTM in all states and the pulsed exit mode switches the DTM back to state S2 and S1 when the LED cools down.

Chapter 5 describes the ASIC design to generate an integrated LED driver with DTM. It begins by giving an overview of current development tools for ASIC design and available design kits including analogue and digital standard cells. For this work the Cadence IC design tool combined with ams hitkit H35 was identified to be most suitable. After introducing the AMS workflow of Cadence IC, the development of the analogue part of the ASIC is shown. It consist of the same elements as the extension board of the discrete implementation, the pre-amplifier for current and voltage measurement and the ADCs for both. The used ADCs and OP-AMPs are part of the analogue standard cells provided from ams. The second part of the ASIC design is the digital implementation including the current and controller, temperature determination and DTM. Due to the slightly different behaviour, constants and coefficients were changed according to the new amplification and conversion behaviour. Similar to the discrete design, three temperature determination methods were synthesised. The quadratic approach needs most space with an area of 404 404 μm^2 followed by the linear approach with an area of 327 527 μm^2, the PJTM approach needs the least amount of space with an area of 179 976 μm^2. Finally, the ASIC was surrounded by an I/O ring. It was fabricated using the linear approach because of less space needed in comparison with the quadratic approach and less disadvantages compared to the PJTM.

In chapter 6 the packed ASIC is tested. For this, a test PCB is developed where the needed peripherals are placed on. Part of the PCB is the clock and reset signal generator, the step-down converter, communication interface and the LED. In experimental tests, the internal LED driver is tested by transmitting an 8 bit value via the UART interface. Unfortunately, the internal current and voltage measurement of the ASIC does not work properly. Measured currents and voltages were higher than the actual value. Therefore, the temperature determination of the ASIC identify overheating, consequently the LED current is reduced to a minimum by the DTM. To overcome this behaviour, the DTM is disabled, thus, a step response of the current controller can be acquired. The forward current of the LED is still quite small because of the mismatched current measurement but the resulting step response is similar to results of the discrete controller. The error in the current and voltage measurements results by differences in the internally placed feedback resistors for current and voltage amplification. Unfortunately, the ASIC does not output this values and therefore it is impossible to adapt the temperature determination coefficient to the internal acquired voltage and current.

7.1. Future Prospects

To improve the ASIC design, the internal developement of amplifiers for current and voltage measurement have to be fixed to work. The measure unit of ASICs on the market are calibrated at the final part test to ensure sufficient accuracy. This is not possible for this ASIC because a Non Volatile Memory (NVM) is needed to store the calibration data and no NVM is available via europractice. Furthermore, the internal measured voltage and current needs to be transmitted by the communication interface to allow the right adjustment of the temperature determination coefficients. In the current ASIC the coefficients for the temperature determination are integrated as a constant. Changed values have to be transmitted each time the ASIC looses power. In a next version of the ASIC, the parameters should be placed in a NVM, too. This will allow to calibrate the chip after production not only for current and voltage measurement but also for the temperature determination.

In addition, an ageing monitor can be included into the ASIC. The temperature of the LED and the operation time give information about the current state of the LED and can be used to determine the approximate time to failure of the LED. When the LED overheat due to an external heat source, the characteristic curve of the LED can change. This will change the voltage temperature relation used to determine the current LED temperature. Monitoring the overheating can be used to adapt the coefficients used for the temperature determination in order to improve the long term accuracy.

In the current system, no active cooling is combined with the temperature determination and the DTM. To improve the behaviour and avoid less light output due to heat, the DTM should be redesigned including an output to control active cooling. For each cooling system another controller is needed because the system behaviour changes. The best applicable way is to use a cascaded control. The developed DTM of this work is working internally without using active cooling. A second controller is placed externally receiving the temperature of the LED from the ASIC and using this value to control the cooling system.

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A

Appendix A

A.1. Calibration

The PCB developed for the calibration is shown in Figure A.3 and the used schematic in Figure A.1 as well as board layout in Figure A.2.

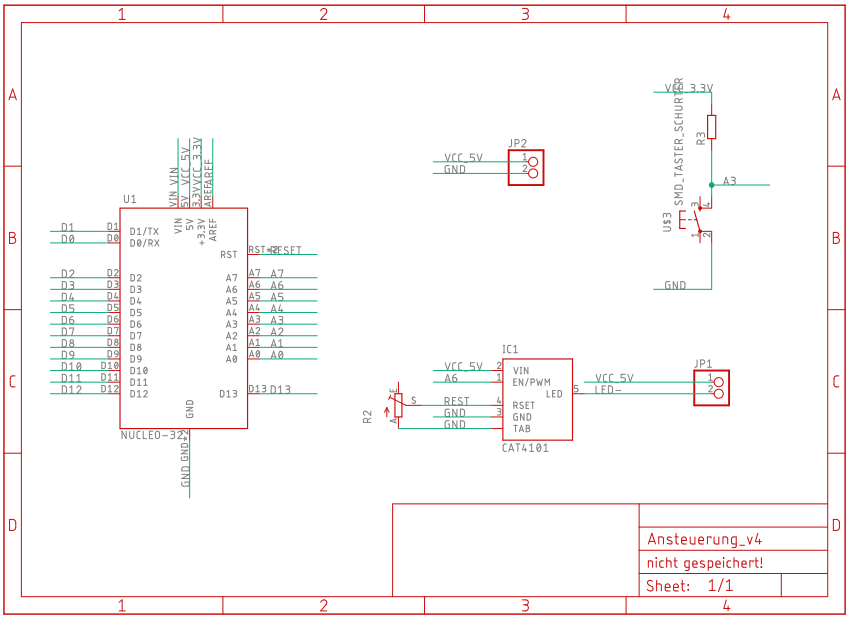
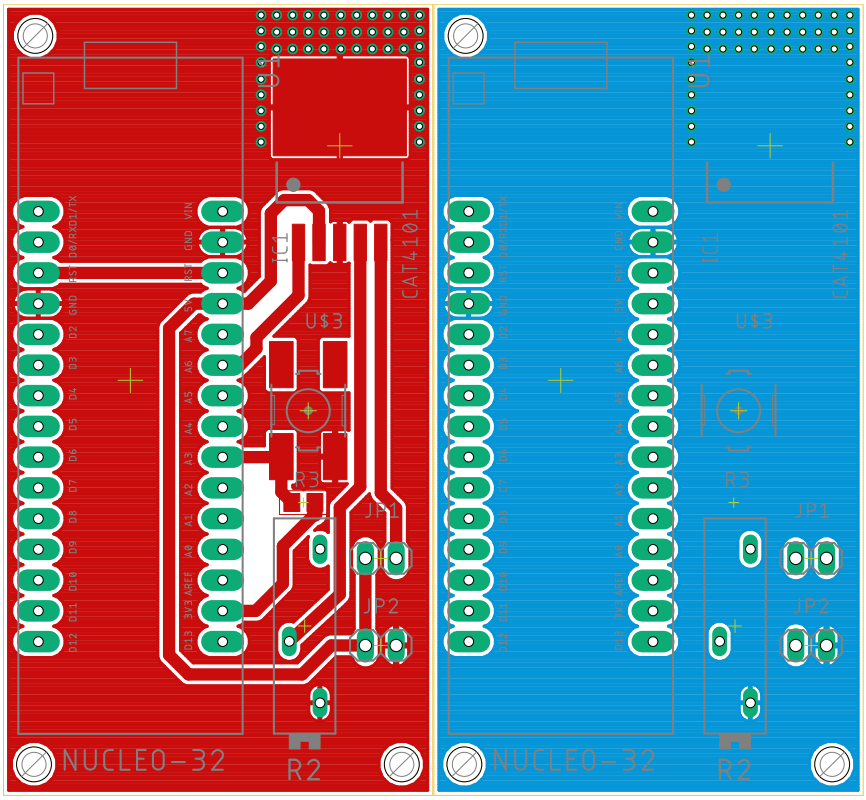


Figure A.1: Schematic of the current pulse PCB

A



(a) (b)

Figure A.2: Board layout of the current pulse generator top (a) and bottom (b)

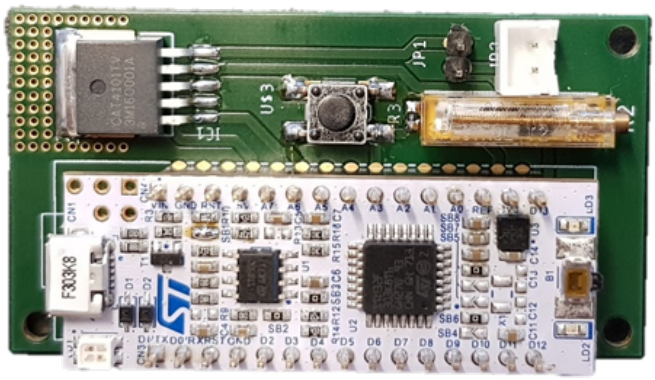


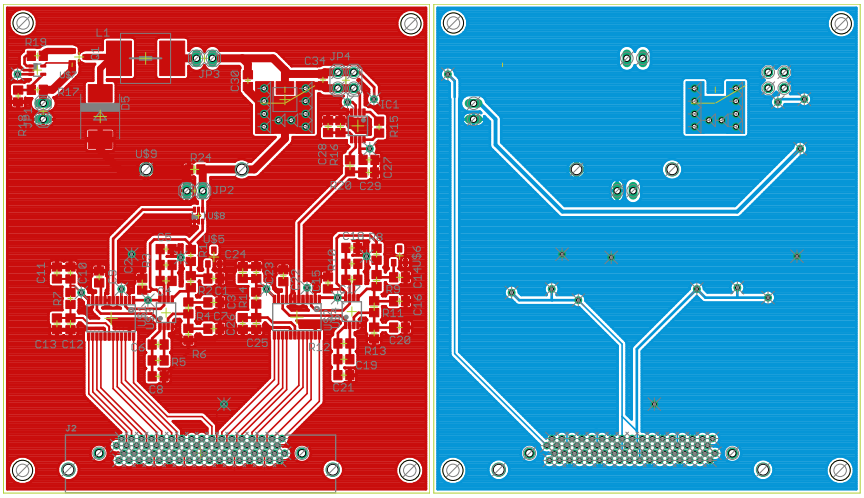
Figure A.3: Picture of the PCB used for the calibration. If the button is pressed, a current pulse of up to 1 A with a length of 20 µs is generated

B

Appendix B

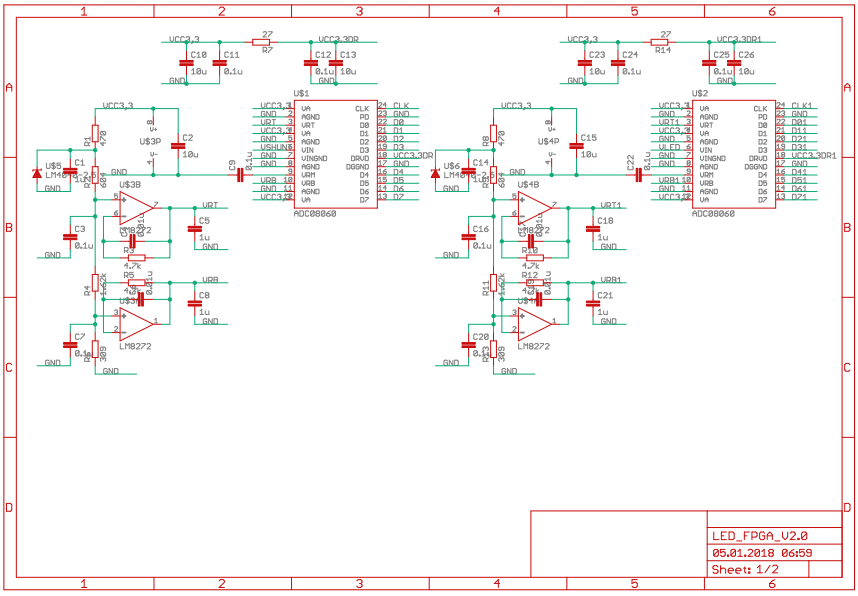
B.1. Discreet implementation

The extension board used for the discrete implementation was designed using EAGLE, following figures show the schematics and the board layout.

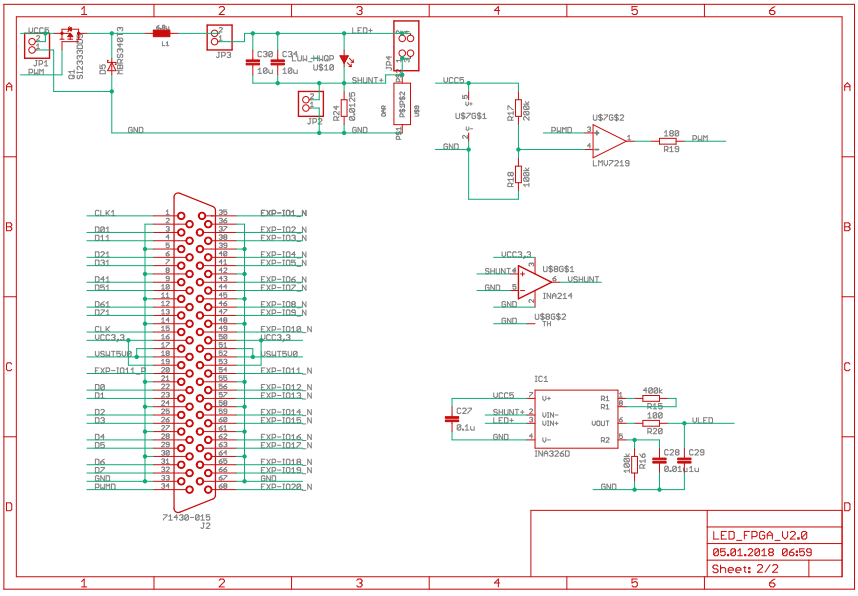


(a) (b)

Figure B.1: Board layout of the extension board for the discrete implementation top (a) and bottom (b)



(a)



(b)

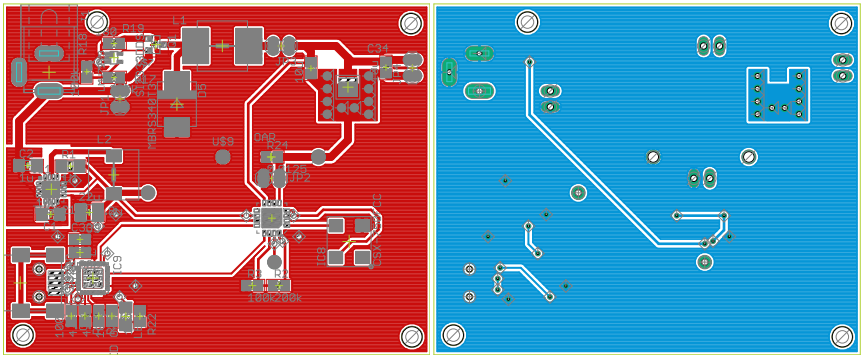
Figure B.2: Schematic of the extension board for the discrete implementation

C

Appendix C

C.1. ASIC implementation

The test board for the ASIC initial operation tests was designed using EAGLE, following figures show the schematics and the board layout.



(a) (b)

Figure C.1: Board layout of the test PCB for the ASIC top (a) and bottom (b)

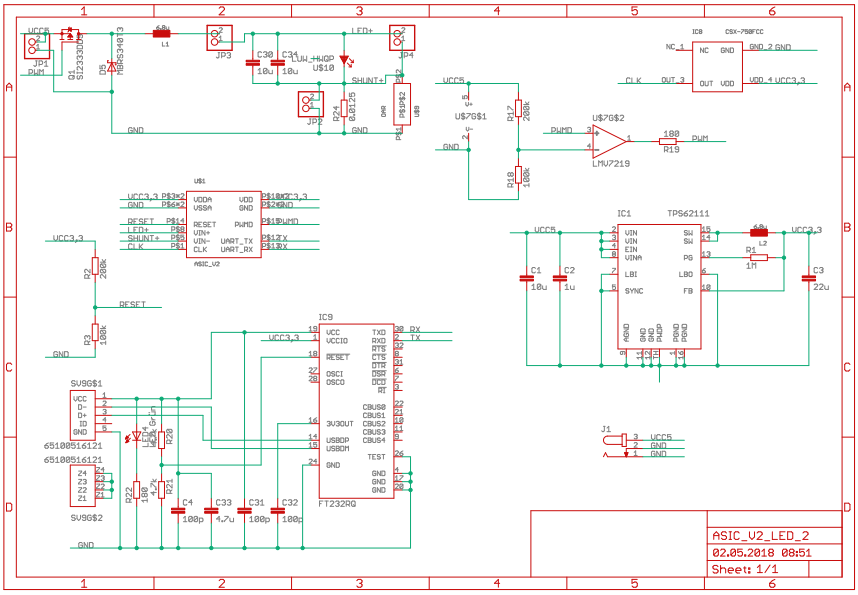


Figure C.2: Schematic of the test PCB for the ASIC